# CrossBar ReRAM Technology

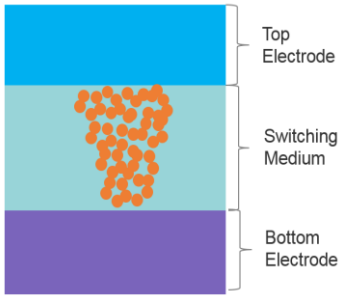
Resistive random-access memory (ReRAM) is widely hailed as the most promising technology in the race to develop new, more scalable, high capacity, high performance and reliable storage solutions.

A typical resistive random-access memory (ReRAM) cell has a switching material with different resistance characteristics sandwiched by two metallic electrodes. The switching effect of ReRAM is based on the motion of ions under the influence of an electric field or heat and the switching material's ability to store the ion distribution, which in turn causes a measurable change in the device's resistance.

There are different approaches to implementing ReRAM, based on different switching materials and memory cell organizations. Those variables drive significant performance differences among the variety of materials being used. The most common challenges for ReRAM technology are temperature sensitivity, integration with standard CMOS technology and manufacturing process and the select mechanism of individual ReRAM cells.

## CrossBar ReRAM Technology Overview

CrossBar ReRAM technology is based on silicon-based switching material as the host material for a metallic filament formation. The resistance switching mechanism is based on the formation of a nanofilament in silicon-based switching material when a voltage is applied between the two electrodes, which makes CrossBar ReRAM cell behavior very stable across a wide temperature range.

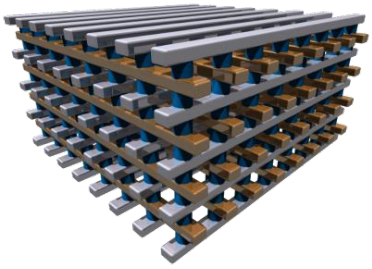



**CrossBar Simple ReRAM Cell**

The resistance switching mechanism of CrossBar's technology is based on the formation of a nanofilament in silicon-based switching material when a voltage is applied between the two electrodes.

Thanks to CrossBar's patented built-in selector, it allows thousands of CrossBar's ReRAM cells to be inter-connected in true cross-point memory arrays. This enables CrossBar cells to be stackable, exhibiting a broad range of device characteristics, and providing high density 3D arrays without occupying additional silicon area. These extremely dense memory arrays with the capability to scale below 10nm, storing multiple bits per cell and stacking 3D layers provide a path towards terabytes on a single die. This feature provides a significant advantage in lowering the cost per gigabit and improving the array efficiency.

In addition to utilizing CrossBar's ReRAM technology in memory applications such as multiple-time programmable (MTP), few-time programmable (FTP) and one-time programmable (OTP) non-volatile memories, this technology can also be used for creating secure cryptographic keys embedded in the semiconductor. These keys are called physical unclonable functions (PUF) keys which are random and unique for every fabricated semiconductor and virtually impossible to reverse engineer or duplicate. The same ReRAM cell technology can be utilized for both memory and cryptographic keys.



**CrossBar 3D ReRAM Architecture**

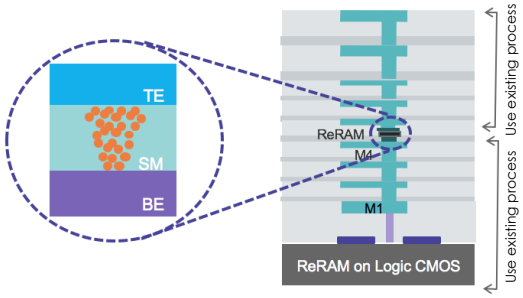
The performance and bits/area density of ReRAM memories depend on the way memory cells are interconnected. Embedded low energy, high performance memory operations for data storage and code execution can be achieved by controlling individually each memory cell with a transistor. In the 1T1R (1 Transistor per 1 ReRAM cell) array organization, the overall memory size is then dominated by the transistor size. High density, low latency storage class memories need a much denser 1TnR memory array organization in which 1 transistor selects thousands of memory cells. The 1TnR organization is possible only if the ReRAM cell has some built-in select mechanism that can individually select or not select specific ReRAM cells.


**CrossBar 1T1R and 1TnR ReRAM Array**

# CrossBar ReRAM Advantages

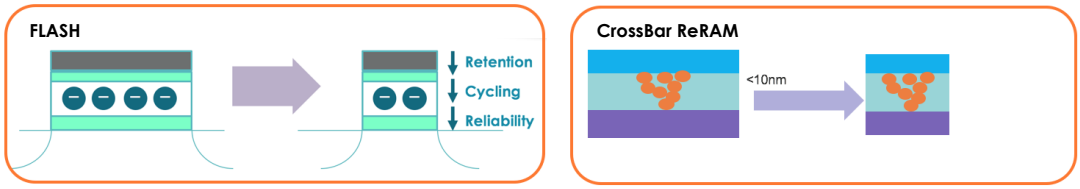
## Manufacturability & Scalability

CrossBar's ReRAM technology is based on a simple device structure using CMOS friendly materials and standard manufacturing processes. It can be easily integrated between two metal lines, directly connected with the underneath CMOS logic IP blocks, and manufactured into existing CMOS fabs without any special equipment or materials. As it is a low temperature Back-End-Of-Line process integration, multiple layers of CrossBar ReRAM arrays can be integrated on top of CMOS logic wafers building a 3D ReRAM storage chip. This enables extremely integrated solutions with on-chip non-volatile memory, processing cores and analog on a single die to provide an elegant and low-cost solution as the most viable alternative to NAND Flash solutions.




**CrossBar ReRAM Standard CMOS Manufacturing**

CrossBar's ReRAM cell operation is based on the storage of a metallic filament in a non-conductive layer compared to electron storage in a Flash memory cell. A few electron losses cause a reliability issue, and retention and cycling become a challenge. This is the reason why Flash memory performance degrades in small process geometries. CrossBar's ReRAM scaling does not impact the device performance and has potential for sub 10nm scaling.




How flash technology scales:
scaling > less electrons > performance degrade

How CrossBar ReRAM technology scales:
scaling > same nanofilament > better performance

**CrossBar ReRAM Scalability**

## Performance

NAND Flash program operation is slow and is done at the granularity of a large page size. Current MLC/TLC NAND or 3D NAND Flash need about 600µs to 1ms to program 8 to 16Kbytes page. NAND Flash has to be erased prior to being programmed. The NAND erase operation is slow, in the 10ms range, and is done for a very large block size, 4-8Mbytes.

The Garbage Collection is an additional layer of data management required to properly free-up blocks with obsolete data when storage is idle. The problem occurs when a new request comes while the garbage collection is moving data from blocks to blocks. This typically introduces long and undeterministic latencies in the range of seconds.

Consequently, SSD writes generally involve writing data more than once between the SSD controller, NAND Flash and DRAM components: initially, when saving the data the first time, and later when moving valid data during multiple garbage collection cycles. As a result, it's common for more data to be written to a SSD's Flash memory than was originally issued by the host system. This disparity is known as write amplification (WA), most systems typically have WA somewhere between 3 and 4. Obviously, write amplification is undesirable because it means that more data is being written to the media, increasing wear and negatively impacting performance by consuming precious bandwidth to the Flash memory. This is especially relevant at smaller process nodes, where the maximum cycle of a NAND memory cell decreases to below three thousand program cycles.

Compared to traditional Flash memory, CrossBar ReRAM is a much faster, bit-alterable, erase-free operation. CrossBar ReRAM technology delivers 100x lower read latency and 1000x faster write performance compared to NAND Flash, and doesn't have the Flash design constraint to build memory arrays in large blocks that can be independently but atomically operated. CrossBar's ReRAM technology can be architected with smaller pages (e.g. 256Byte pages vs. 16KByte pages in NAND) that can be independently re-programmed. This new storage architecture drastically simplifies the complexity of the storage controller by removing a large portion of the background memory accesses required for garbage collection. With a write amplification equal to 1, the benefits to the users are visible in terms of read and write latencies, lower energy consumption and increased lifetime of the storage solutions.

Also, the erase-free architecture with small page granularity that can be re-programmed without a block erase provides an impressive performance boost over Flash-based Solid-State solutions. This also reduces the complexity of the storage controller and reduces the number of background memory accesses enabling a new era of Solid-State data storage solutions.

Next-generation SSD controllers optimized for ReRAM will be able to update smaller pages faster and drastically reduce the background memory operations required for NAND. ReRAM-based SSD will provide lower and more deterministic read latencies, in the range of tens of µsec.

## Density

CrossBar's patented selector device solves one of the greatest technical challenges faced by developers of high-density ReRAM called the sneak current (or leakage current). CrossBar's 3D ReRAM storage solutions are based on 1TnR arrays (1 Transistor driving n Resistive memory cell), selectivity making it possible for a single transistor to manage a very large number of interconnected memory cells, which enables very high capacity solid-state storage. While 1TnR enables a single transistor to drive over 2,000 memory cells with very low power, it also experiences leakage of a sneak path current that interferes with the performance and reliability of a typical ReRAM array. CrossBar's patented field assisted superlinear threshold device is the industry's first selector capable of suppressing the leakage current below 0.1nA and has been successfully demonstrated in a 4 Mbit integrated 3D stackable passive CrossBar array.

CrossBar's selector solves the sneak path problem by achieving the highest reported selectivity of 10^10, as well as an extremely sharp turn-on slope of less than 5mV/dec, fast turn-on and recovery (<50ns), an endurance greater than 100M cycles, and a processing temperature less than 300°C, all ensuring commercial viability. CrossBar's selector is the first solution to overcome this design challenge, paving the way for terabyte storage-on-a-chip to become a reality and positioning ReRAM as the leading next generation NAND memory replacement.

## Energy

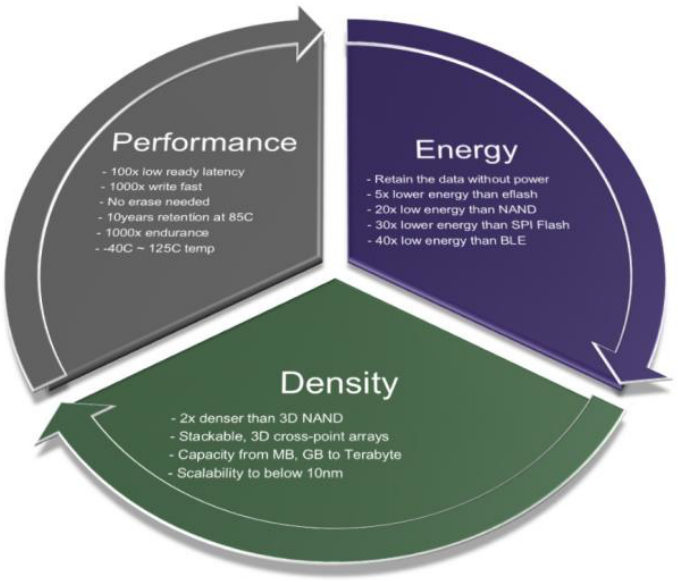
CrossBar's ReRAM technology will simplify the management of data writes and data reads between the multiple data storage components and the controller within a SSD or other similar data storage solution. Reducing the number of background memory operations improves the performance and overall endurance of the data storage solution but also reduces the overall power consumption of both the SSD controller, the DRAM usage, and the read and write power budget consumed by the data storage components.

At the memory cell level, CrossBar's ReRAM improves programing performance and power consumption by achieving a 64pJ/cell program energy, a 20X improvement compared to NAND Flash technology.

Other advantages of CrossBar's 3D ReRAM include 1M+ write cycle endurance, 10years @85C retention, simple controller due to erase-free operation, and byte-level overwrite capability. Since MTP, FTP and OTP memories and PUF keys are able to share a monolithic ReRAM manufacturing process and control circuity, a single chip design can now support custom chips by dynamically re-sizing memory during test time, offering CrossBar business partners additional flexibility.

## ReRAM For PUF Security

CrossBar has announced the usage of its Resistive RAM based technology for use as physical unclonable function (PUF) cryptographic keys. Today, semiconductor companies exploit the characteristics of SRAM memory (Static Random Access Memory) embedded in semiconductors to produce a unique set of keys or "fingerprint" for each chip to improve secure operation. This technology has numerous weaknesses limiting its effectiveness including poor key randomness, high bit error rates, limited tamper resistance and longer sensing times. In contrast, CrossBar's new ReRAM PUF key technology is enabling a new class of secure devices and systems, addressing the deficiencies related to SRAM PUF.




**CrossBar ReRAM Advantages**

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CrossBar is the leader in ReRAM technology, enabling kilobytes to terabytes of always-on data storage to be embedded into any processor, microcontroller, FPGA or as a standalone memory chip. CrossBar ReRAM lets designers rethink the compute/storage paradigm, free from the constraints of traditional flash and DRAM memories. From “persistent memory” that brings data closer to CPU to “cognitive memory” that enables in-memory computing without a host CPU, ReRAM is ushering in new era of data storage and processing for both edge and cloud computing. For more information, visit www.crossbar-inc.com.