

3D-stackable Crossbar Resistive Memory based on Field Assisted Superlinear Threshold (FAST) Selector

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Abstract

We report the integration of 3D-stackable 1S1R passive crossbar RRAM arrays utilizing a Field Assisted Superlinear Threshold (FAST) selector. The sneak path issue in crossbar memory integration has been solved using the highest reported selectivity of 10^{10} . Excellent selector performance is presented such as extremely sharp switching slope of $< 5\text{mV/dec.}$, selectivity of 10^{10} , sub-50ns operations, $> 100\text{M}$ endurance and processing temperature less than 300°C . Measurements on the 4Mb 1S1R crossbar array show that the sneak current is suppressed below 0.1nA , while maintaining 10^2 memory on/off ratio and $> 10^6$ selectivity during cycling, enabling high density memory applications.

Introduction

For ultra-high density nonvolatile memory applications ($>1\text{Tb}$), 3D-stackable 1TnR or 1S1R structures is needed. Suppressing the leakage (sneak) current in 1TnR or 1S1R crossbar arrays has been a main challenge for high density RRAM development. Various selector devices such as tunneling diode [1], bidirectional varistor [2], MIEC [3] and Ovonic threshold switch [4] have been proposed. Key requirements of selectors include high selectivity ($\Delta I @ V_R, 1/2V_R$), steep turn on slope, high current density, fast turn on and recovery and high endurance. Previous reported selector devices showed selectivity of $150 \sim 10^5$ and turn on slope of $60 \sim 450\text{mV/Dec}$. In this work, we present a FAST selector with selectivity of $\sim 10^{10}$, turn on slope $< 5\text{mV/dec}$, fast turn on and recovery ($< 50\text{ns}$). Furthermore, 4Mb 1S1R RRAM arrays are demonstrated with large memory on/off ratio and selectivity.

Selector Device

The FAST selector utilizes a superlinear threshold layer (STL) in which a conduction path is formed at the threshold

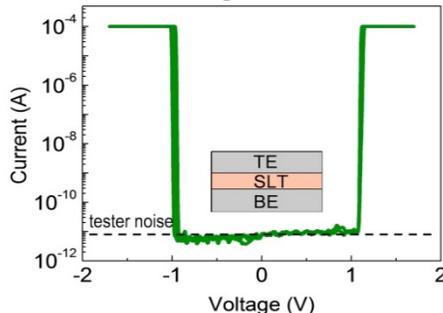


Fig. 1. I-V characteristics of FAST selectors (100nm x 100nm). The device shows bidirectional threshold switching with larger than 10^7 on/off ratio (test-limit).

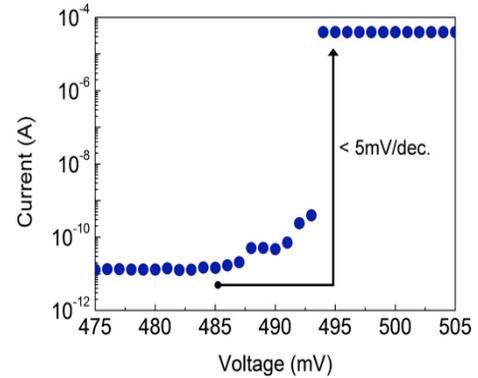


Fig. 2. Zoomed-in plot showing the turn on slope of the FAST selector. The device showed extremely sharp turn on slope of less than 5mV/dec .

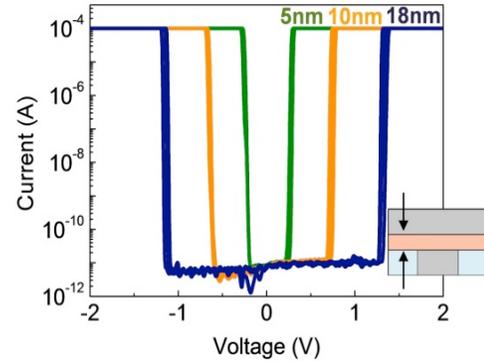


Fig. 3. The threshold voltages can be tuned by controlling the SLT layer thickness.

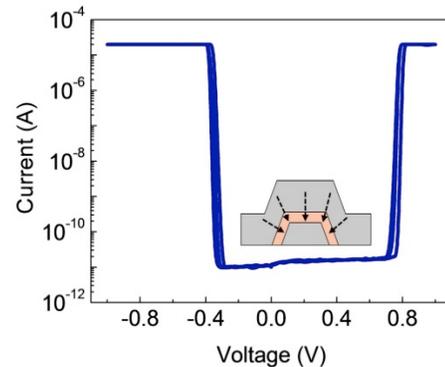


Fig. 4. Asymmetric threshold voltages can be achieved by modulating the device structure (by the modulation of electric field).

electric field. The device provides bidirectional volatile switching with large resistance ratio, high turn on current and steep turn on slope, as shown in Fig. 1. The measured selectivity for the $100\text{nm} \times 100\text{nm}$ device is $> 10^7$, and is limited by the test setup. The switching slope is extremely sharp and is less than 5mV/dec . (Fig. 2), which is

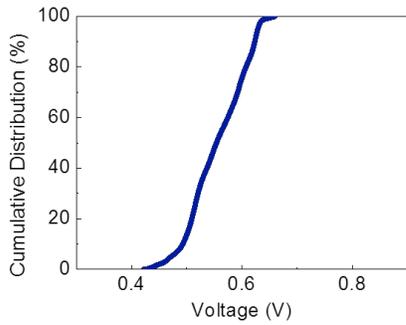


Fig. 5. Threshold voltage (V_{TH}) distribution of FAST selectors within a wafer. Target V_{TH} : 0.6V.

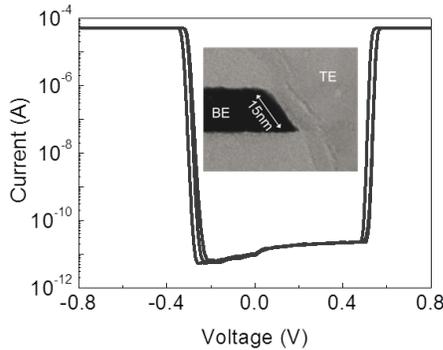


Fig. 6. Reliable switching was still maintained in 15nm x 100nm devices.

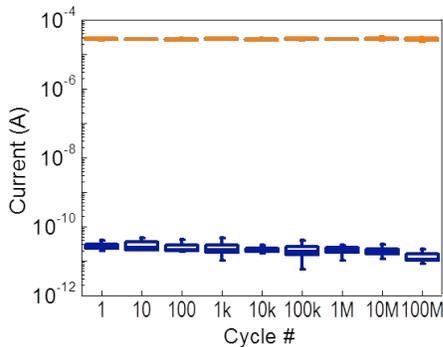


Fig. 7. Cycling test of FAST selectors. The selectors can be reliably cycled over 100M cycles while maintaining $> 10^6$ on/off ratio (test limited).

beneficial to array level operations (e.g. larger read voltage margin, faster read). The threshold voltages (V_{TH}) of the selector can be tuned by controlling either the STL thickness or device structure (Figs. 3-4). Fig. 5 shows good device uniformity and tight V_{TH} distribution. Reliable switching can be maintained in 15nm x 100nm devices (Fig. 6) with current density $> 5 \times 10^6 \text{A/cm}^2$. The selector can reliably switch over 100M cycles (Fig. 7). To test disturb at half-selected bias, a constant DC stress at $0.5V_{TH}$ was applied for a two hour-long period, which did not turn-on the device (Fig. 8). For voltage above V_{TH} , the switching speed is faster than 50ns with the on-off transition time less than 5ns (Fig. 9). The device can quickly recover to the off state once the voltage is removed, with a recovery time $< 50\text{ns}$ (Fig. 10). Once a device switches

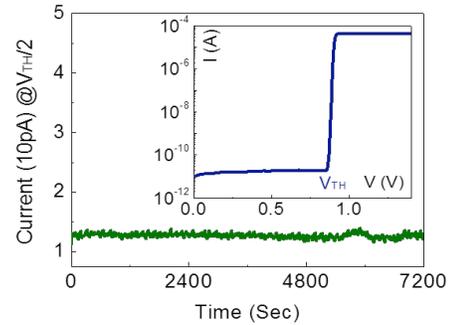


Fig. 8. DC stress test. The device did not turn-on at $0.5V_{TH}$ during two hour-long DC stress. Inset: DC switching characteristic.

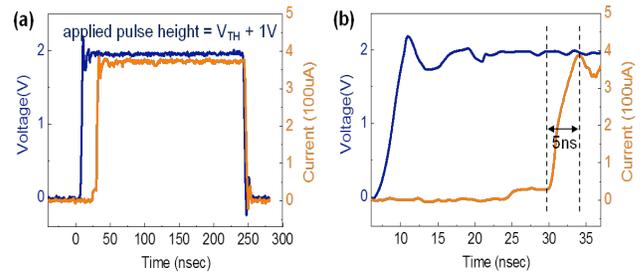


Fig. 9. Switching speed of a FAST selector. (a) The selector can be turned-on within 30ns in response to a 2V pulse. (b) Zoomed-in figure of (a). Off-to-on transition time is about 5ns (tester limited) for over 300uA of passing current through the selector.

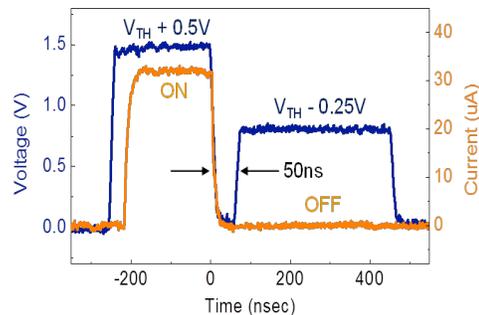


Fig. 10. The selector quickly relaxes to the off state in less than 50ns.

to the on-state, a much smaller hold voltage (V_H) is required to deliver a target current I_p (Fig. 11 (a)). V_H increases as I_p increases, but it was found to be independent of V_{TH} (Fig. 11 (b)-(d)). The small ($< 0.3\text{V}$ for 200uA) V_H and very large off-state resistance minimize the voltage overhead when integrated with RRAM.

Array Integration

The FAST selectors have been integrated to a passive crossbar array (Fig. 12). Even for a 4Mb crossbar array, the sneak current has been suppressed below 0.1nA at both 25°C and 125°C, demonstrating very high device yield and low leakage current. We have also successfully integrated the FAST selectors with RRAM in passive crossbar 1S1R arrays.

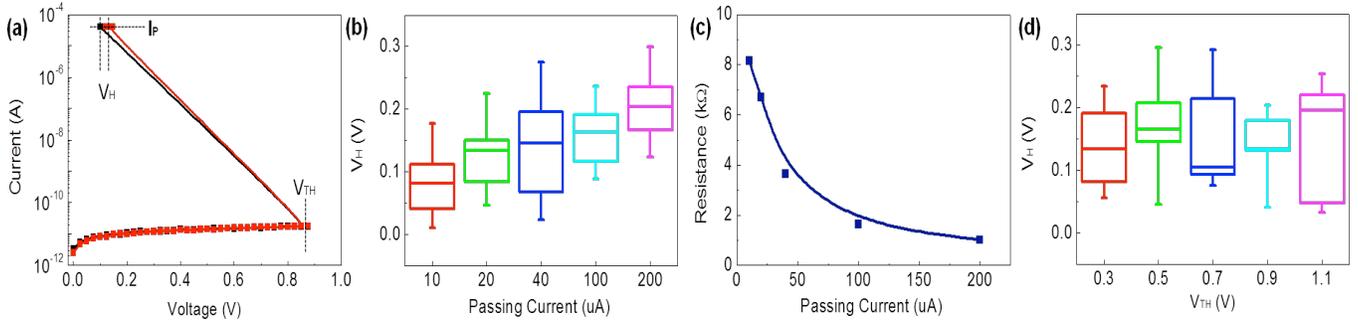


Fig. 11. Hold voltage (V_H) characteristics of FAST selectors. (a) Once a device switches on, a small V_H is required for passing a specific target current (passing current I_p). (b) I_p vs. V_H . (c) Median on resistances vs. I_p . (d) V_{TH} vs. V_H .

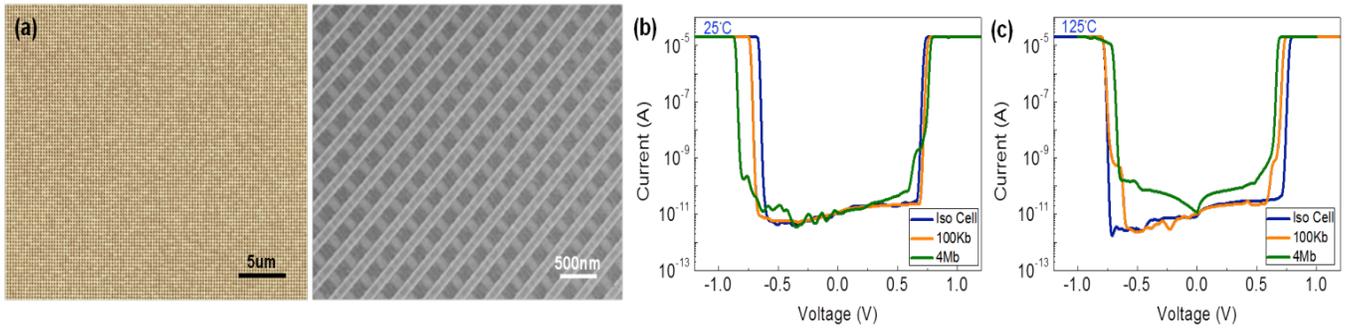


Fig. 12. Passive crossbar array integration of FAST selectors (single cell to 4Mb array). (a) Images of the fabricated selectors. (b) I-V characteristics of the integrated selectors (isolated single cell, cells in 100Kb and 4Mb arrays) at 25°C. (c) I-V at 125°C.

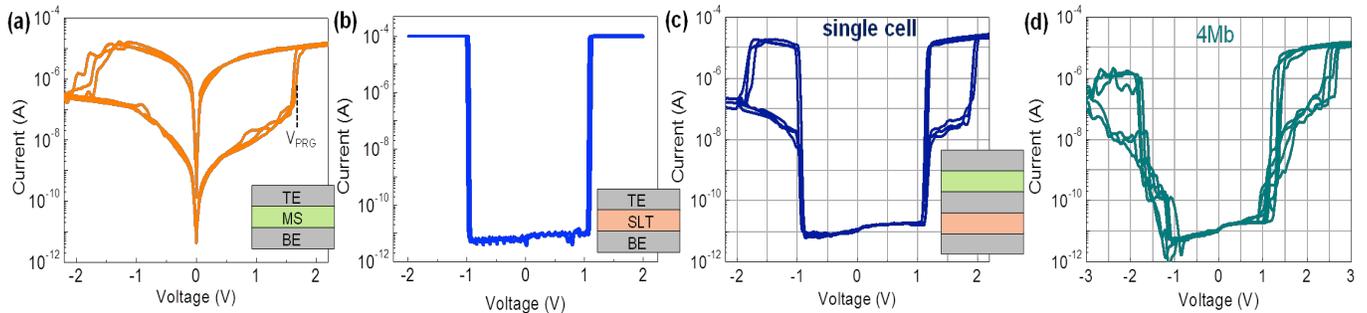


Fig. 13. Passive crossbar integration of RRAM devices with FAST selectors. I-V characteristics of a single cell level (a) RRAM, (b) selector, and (c) integrated 1S1R device. (d) I-V characteristics of a 4Mb passive crossbar array based on 1S1R.

For large array integration, we developed forming-free low current ($\leq 20\mu\text{A}$) RRAM cells (Fig. 13 (a)) to minimize IR drop and power consumption, and we designed selectors of which V_{TH} is larger than $0.5V_{PRG}$ but smaller than V_{PRG} (Fig. 13 (b)) of the RRAM to suppress sneak currents during both the program and the read operations. The integrated 1S1R device shows $> 10^2$ memory on/off ratio and $> 10^6$ selectivity (Fig. 13 (c)). The device operations can be also maintained for the 4Mb 1S1R crossbar arrays (Fig. 13 (d)), which is the largest array size demonstrated to date in a passive crossbar structure. The integrated device can reliably switch more than

100K cycles while maintaining the large memory on/off and selectivity (Fig. 14). To extract the intrinsic leakage current of an individual selector, leakage current through an entire 40Kb selector array was measured (Fig. 15 (a)). The extracted selectivity is found to be 10^{10} (@100nm device). Fig. 15 (a) also shows that there is no single shorted selector device within the 40Kb array. By using the same test method, we calculated the selectivity for different device areas (Fig. 15 (b)). Circuit simulations showed that the selectivity larger than 10^5 is required to design Mb level passive crossbars (Fig. 16) and our FAST selectors surpass the requirement.

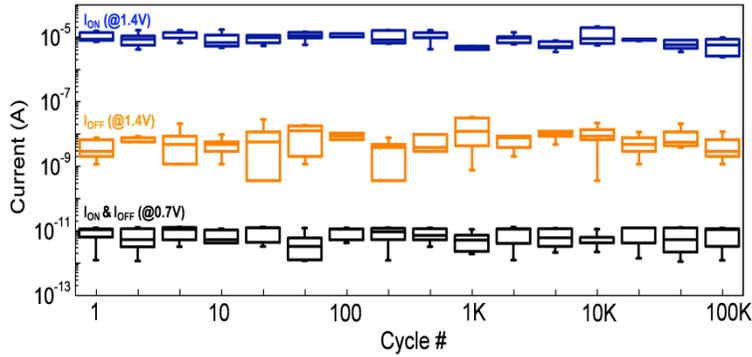


Fig. 14. Cycling demonstration of 1S1R devices. On, off states and half-selected currents are shown. The integrated 1S1R devices maintained $> 10^2$ memory on/off ratio and $> 10^6$ selectivity during the cycling.

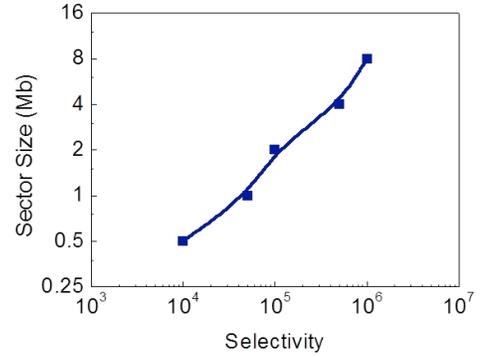


Fig. 16. Practical passive crossbar sector size vs. selectivity. Assumed concurrent 2kb program with $I_{cc\ max} = 50mA$.

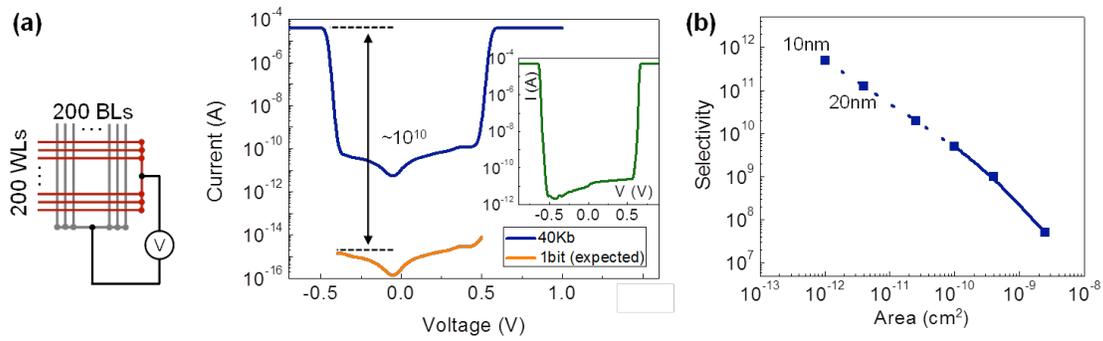


Fig. 15. Leakage current test of selectors and the projected selectivity. (a) Leakage current through entire 40Kb devices and projected 1bit (100nm x 100nm) leakage current. Inset: Typical I-V of a selector on the same wafer. (b) The selectivity vs. device area based on the leakage current measurement.

Table 1. FAST selector summary

| Key Parameters | Performance |
|---------------------------------------------|--------------------------------------------------------------|
| Selectivity ($\Delta I @ V_R, 1/2V_R$) | $\sim 10^{10}$ (@100nm) $\geq 10^{11}$ (@20nm, projected) |
| Endurance | $> 10^8$ |
| Voltage overhead (Hold voltage) | $< 0.3V$ for passing 200uA |
| Switching slope | $< 5mV/dec.$ |
| Max. current density | $> 5 \times 10^6$ A/cm ² |
| Processing Temp. | $< 300^\circ C$ |

Conclusion

As summarized in Table 1, FAST selectors offer excellent performance metrics such as the largest reported selectivity (10^{10}) to date, steep slope and fast turn on/recovery for high density memory applications. Functional 4Mb passive crossbar RRAM arrays have been demonstrated based on the FAST selectors.

References

- [1] A. Kawahara et al., IEEE ISSCC, 25.6, 2012
- [2] W. Lee et al., VLSI Tech. Symp., 37-38, 2012
- [3] K. Virwani et al., IEDM, 36-39, 2012
- [4] S. Kim et al., VLSI Tech. Symp., T240-241, 2013