RRAM enabling new Era of Solid State Storage Arrays

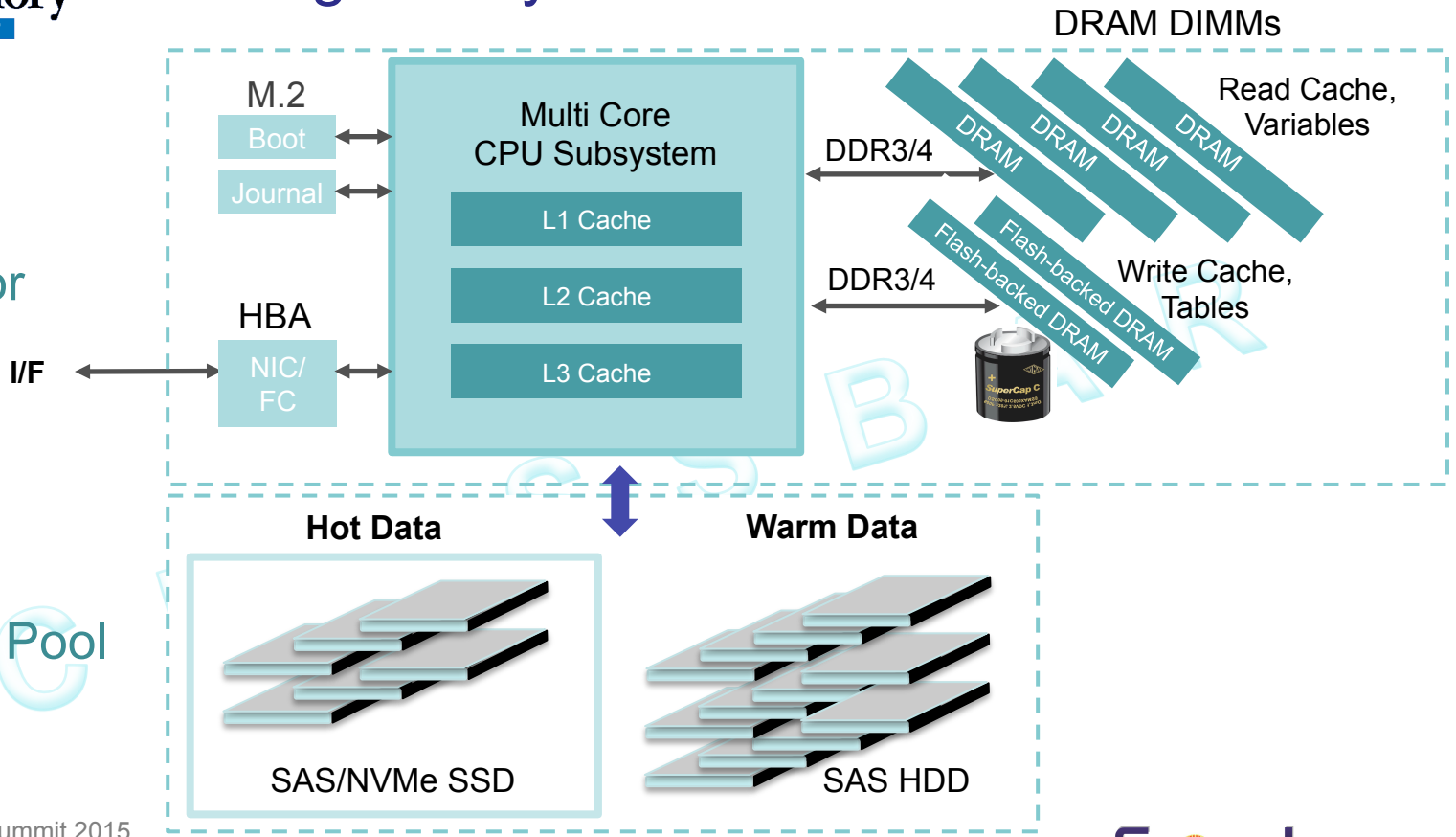
Mehdi Asnaashari
Chief System Architect, Crossbar Inc.

Changing Memory Landscape

- NAND memory has revolutionized Storage in the past 20 years
- All-NAND Storage Arrays/Appliances have thrived in the past few years
- BUT as we all know, NAND has its own deficiencies

How Can Resistive Memory Change Storage Array Landscape?

Storage Array **TODAY**



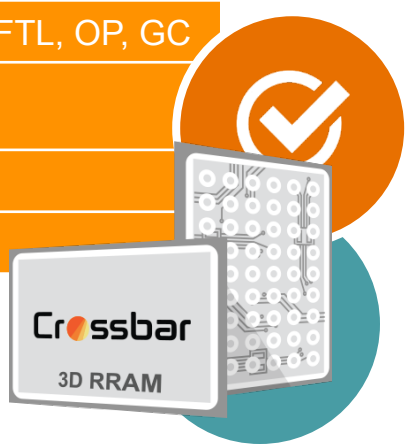
But NAND Has Its Deficiencies

Disadvantages

PAGE PROGRAM operation is slow (~1 ms)
BLOCK ERASE operation is very slow (~10 ms)
READ LATENCY is ~100us
1,500 PE cycles
No Over-write, forcing Write Amplification
Large page size of 16-32KB
3 years data retention @ 25C
Severe scaling limitation

Crossbar RRAM Memory Overcomes NAND Deficiencies

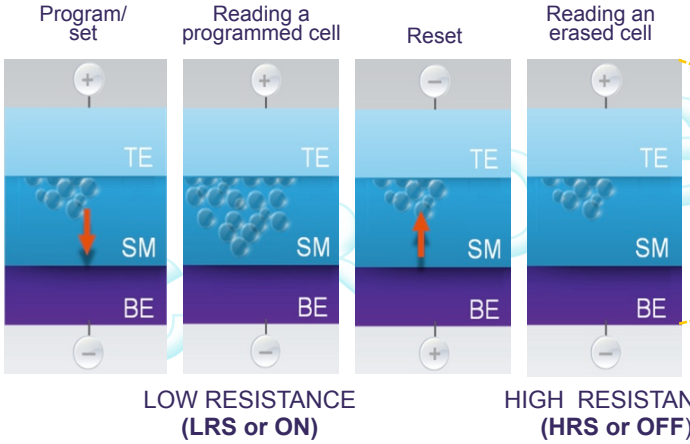
Disadvantages	Crossbar RRAM Advantages
PAGE PROGRAM operation is slow (~1 ms)	PAGE WRITE operation is very fast (~2 us)
BLOCK ERASE operation is very slow (~10 ms)	No BLOCK ERASE operation
READ LATENCY is ~100us	READ LATENCY of 1us
1,500 write cycles	100K write cycles
No Over-write, forcing Write Amplification of ~3	Allows Over-Write of data; WA=1, no FTL, OP, GC
Large page size of 16-32KB	Small page size of 256-512B
3 years data retention	10 years data retention
Severe scaling limitation	Scales below 10nm



Crossbar's RRAM Technology

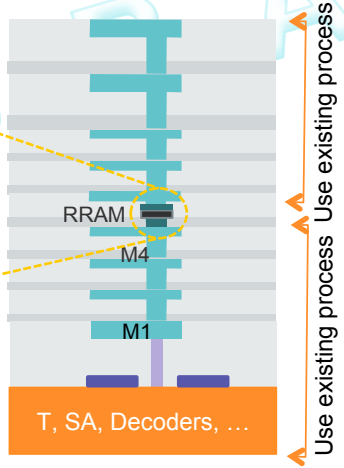
Crossbar RRAM Cell

- Simple device structure using fab friendly materials and process
- Information is stored in the form of metallic nano-filament in a non-conductive layer
- Filamentary-based switching by electric field



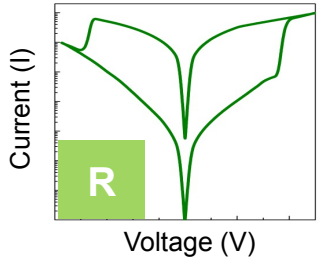
CMOS Integration

- Standard semiconductor manufacturing equipment
- Low temperature Back-End-Of-Line standard CMOS integration
- RRAM cell between two metal lines



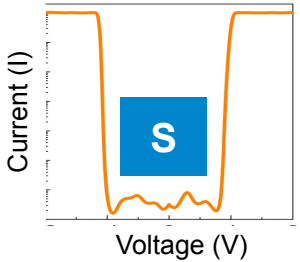
Crossbar Technology – Achieving High Density

RRAM



(a)

Crossbar Select



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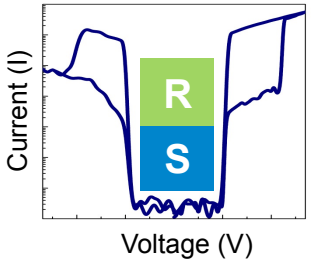
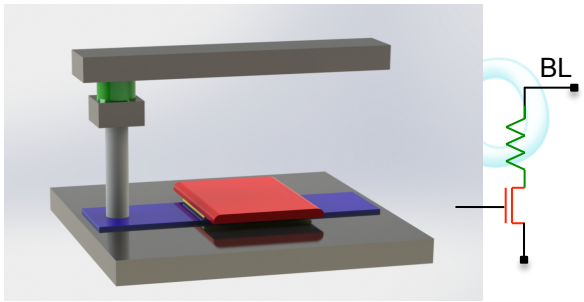
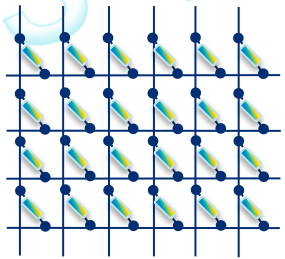
SR

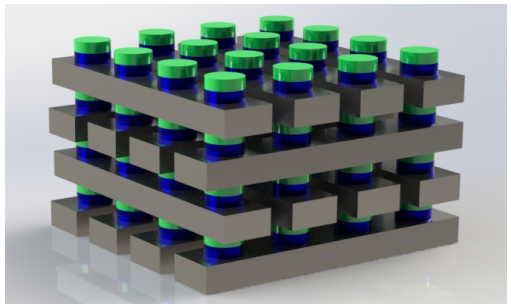


(c)



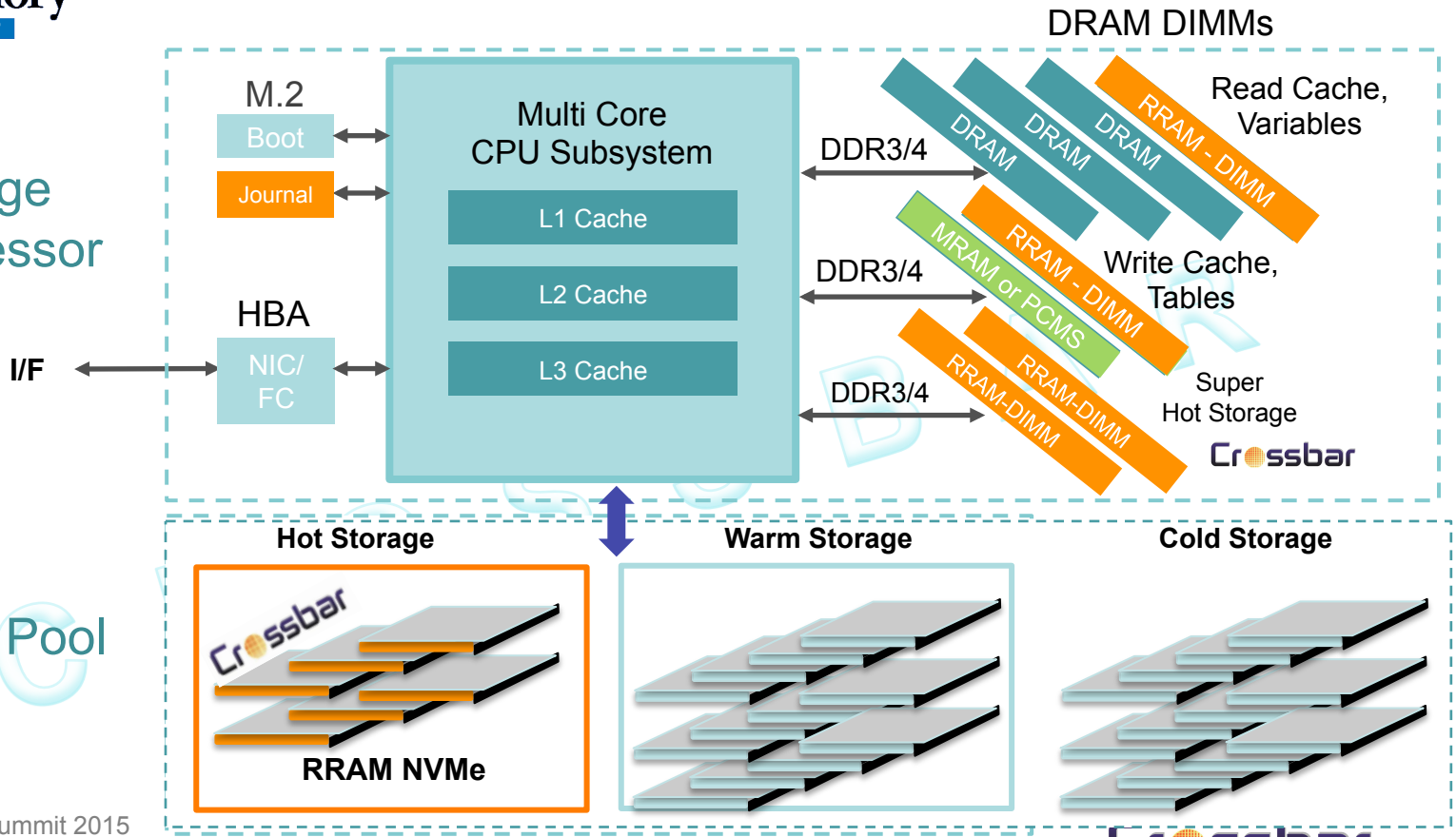
1T1R





1TnSR with n=1000's

Storage Array in 2 years



What Can an RRAM based DIMM Module DO?

RRAM

- **ONFI 4 Interface**
  - 800 MT/S
- **1us Read Time**
- **2us Program Time**
- **No-Erase Required**
- **Multi-Bank Architecture**

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Controller

- **64-bit DDR3 IF**
  - 1600 MT/s
- **16 ONFI 4 Channel BE**
  - 800 MT/s
- **ECC**
- **No External DRAM**

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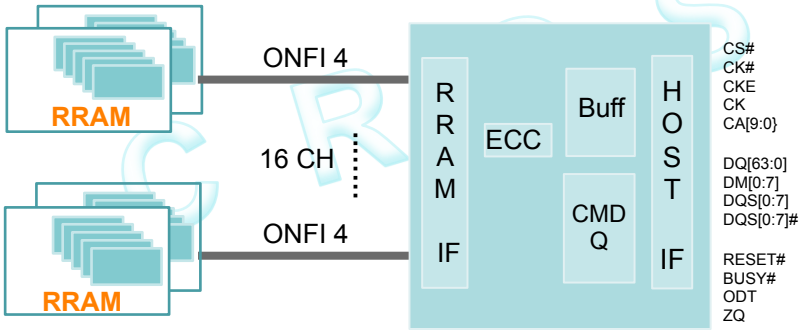
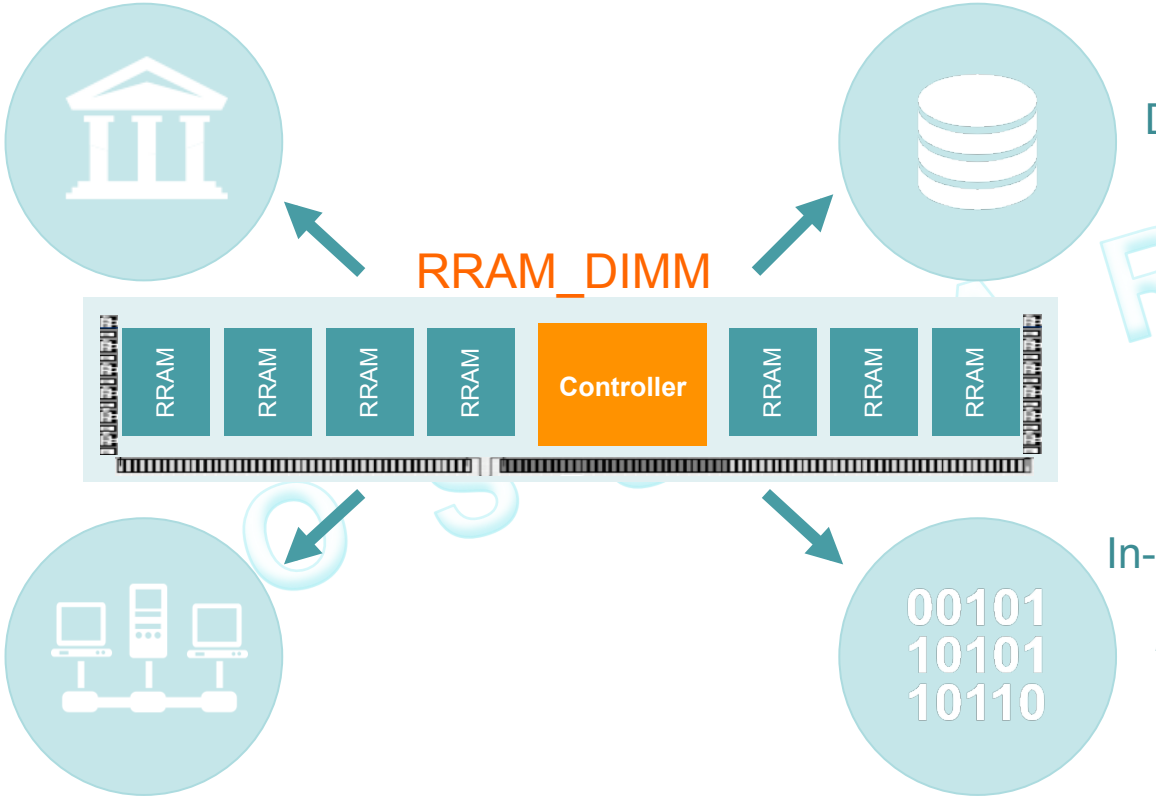
DIMM Module

- **Interface: 64-bit DDR3 800 MHz**
- **Read Performance**
  - **Random Read Latency: 4us (Max)**
  - **3 Million Random 4K IOPs**
  - **24 Million Random 512B IOPs**
- **Write Performance**
  - **Write latency: 4us (Max without caching)**
  - **3 Million Random 4K IOPs**
  - **24 Million Random 512B IOPs**
  - **No Erase prior to Write command**
- **Endurance: 10^5 Write cycles**

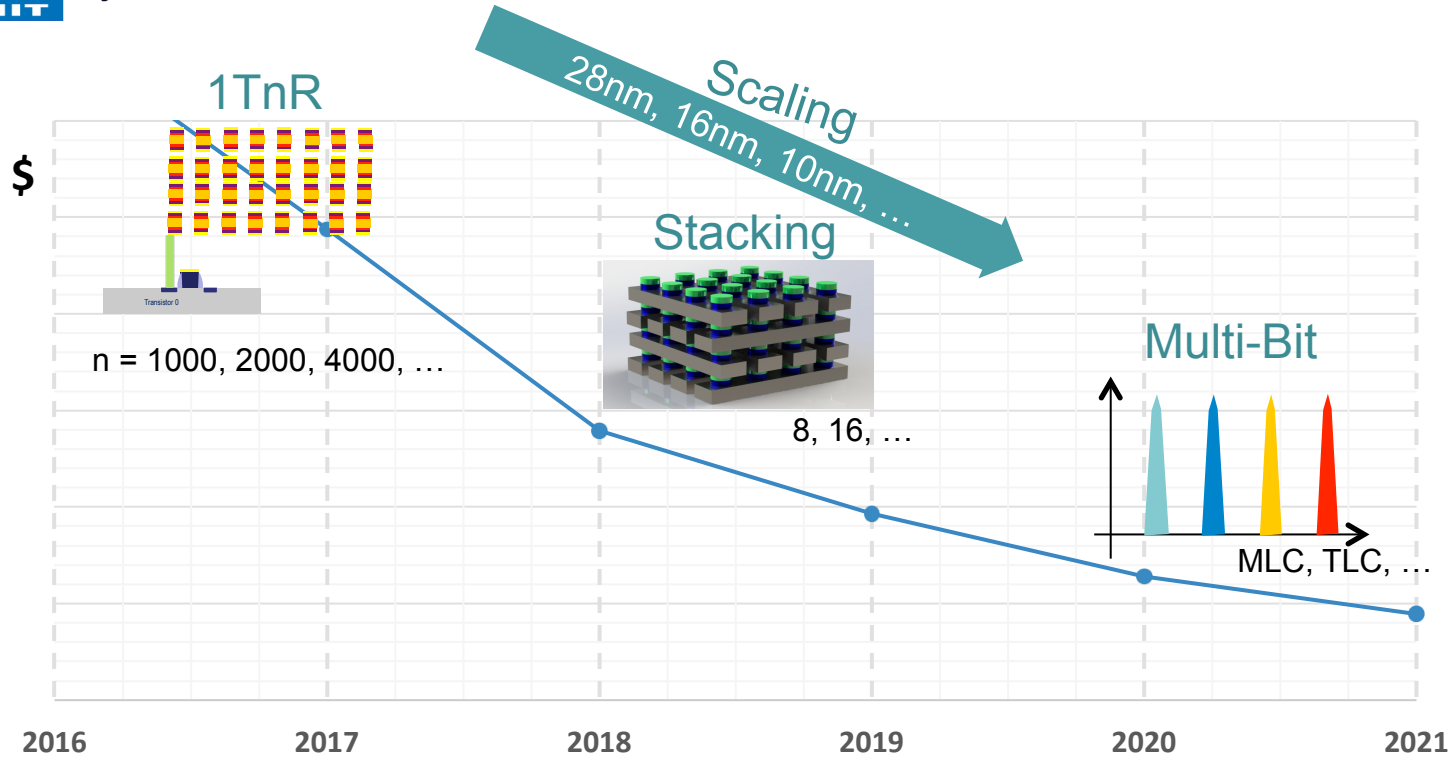
Block Diagram



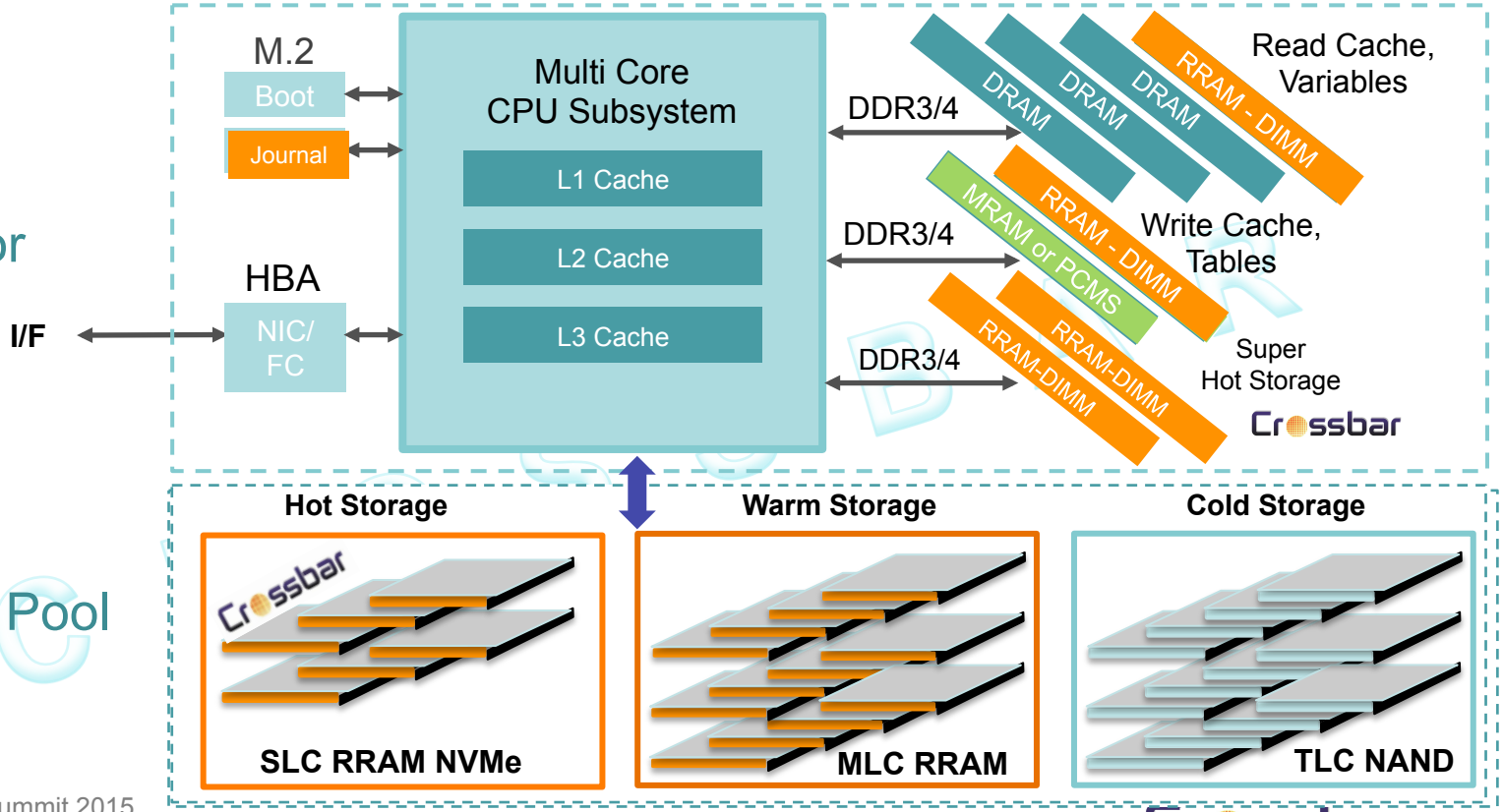
Applications Benefiting from RRAM-DIMM



RRAM Moving Forward

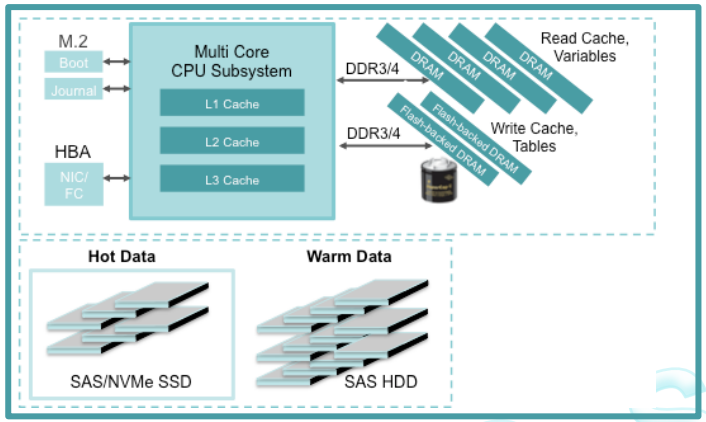


Storage Array in 5 years

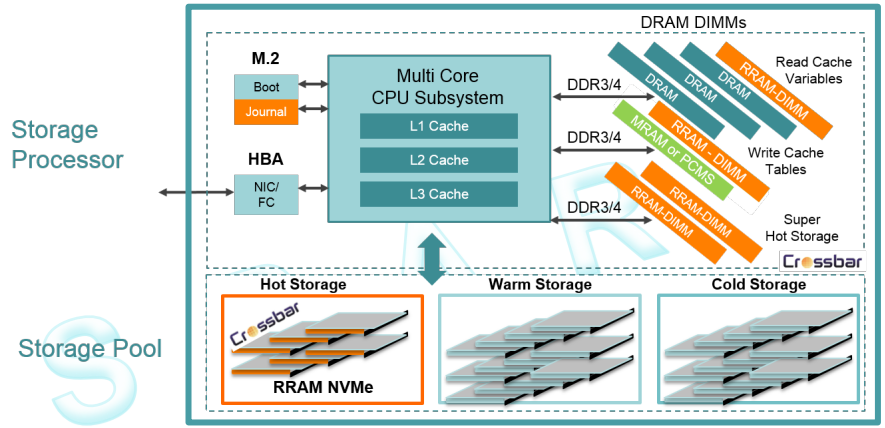


Storage Array Comparison

NAND Based Storage Array



RRAM Based Storage Array



2 Million IOPs

> 20 Million IOPs

25X Lower Read Latency
>10X Higher IOPs
5X Longer Lifetime @ 20 M IOPs

New Era for Enterprise Storage Architecture

- One RRAM device can fully saturate an ONFI 4 Bus
- 10's of Millions of IOPs in a real estate constraint system
- 100's of Millions of IOPs in a storage array
- Burden has shifted from Storage to Host/Application to generate the IOs
- How can all these IOPs be harvested effectively?
- Perhaps it's time for Distributed Computing and Micro Servers/Blades
  - Dedicated computing engines with each having 100's of GBs of Storage
  - More complex commands; query, …

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