

Breakthrough 3D RRAM

Technology for super-dense, low latency,
low power data storage systems

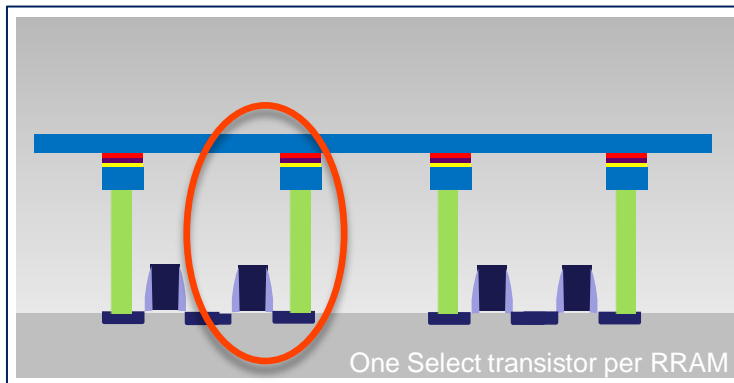
Hagop Nazarian

Co-Founder VP Engineering, Crossbar Inc.

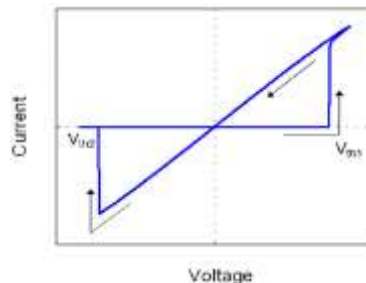
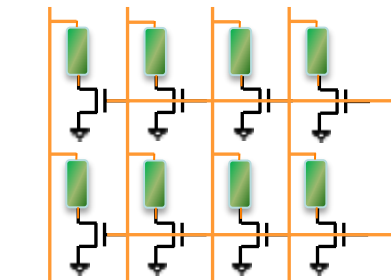
- **Introduction**
- **Architectural RRAM Classification**
- **The Sneak Path Barrier**
- **Crossbar RRAM with High Selectivity Ratio**
- **Crossbar 1TnR characteristics & benefits**
 - Area vs selectivity ratio
 - Power vs selectivity ratio
 - Latency vs 1TnR architecture
- **Summary**

Architectural RRAM Classification

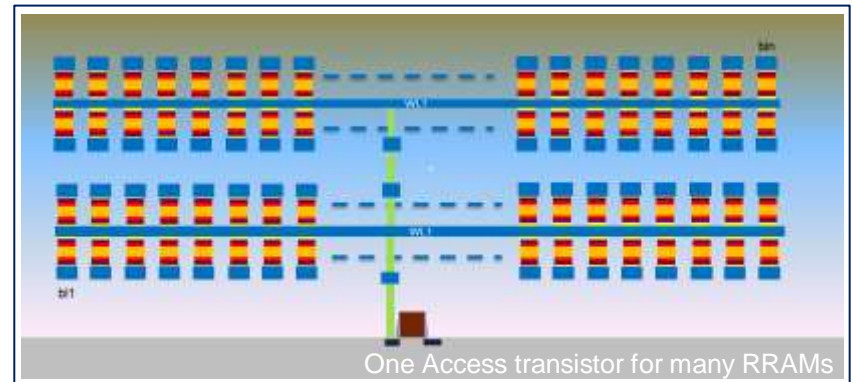
1T1R with Linear RRAMs



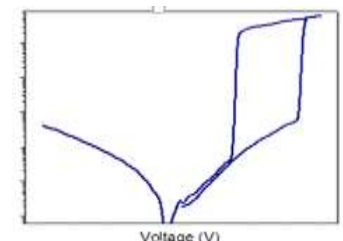
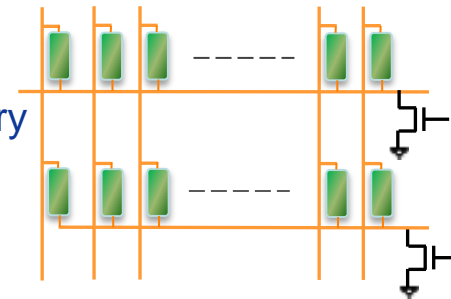
- Suited for low latency, high speed embedded memory operation or high performance NOR products
- Cell size dominated by the select transistor



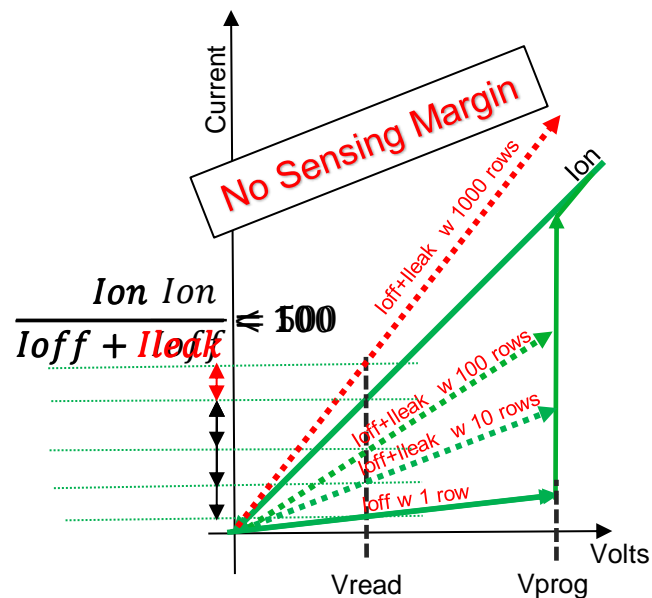
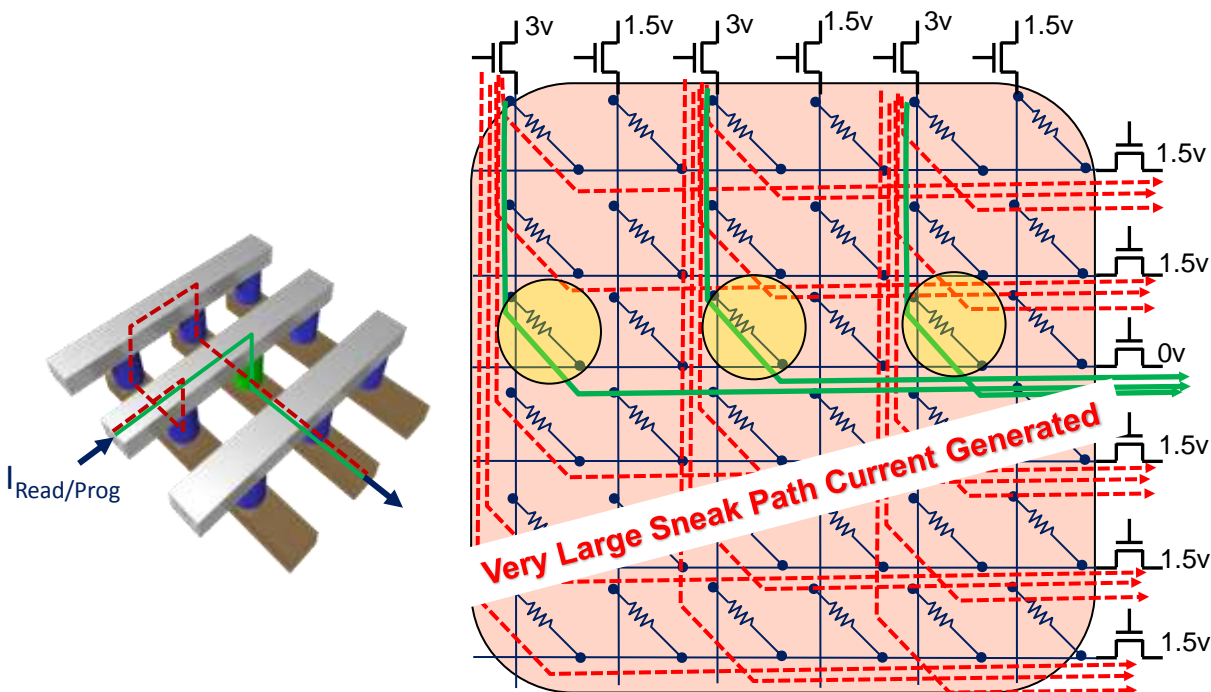
1TnR with Non-Linear RRAMs



- Suited for high density high performance memory (NAND/SCM memory)
- 3D architecture
- Under array utilized for peripheral circuits yielding high array efficiency
- $$\text{Cell area} = \frac{4F^2}{\# \text{ RRAM Layers}}$$

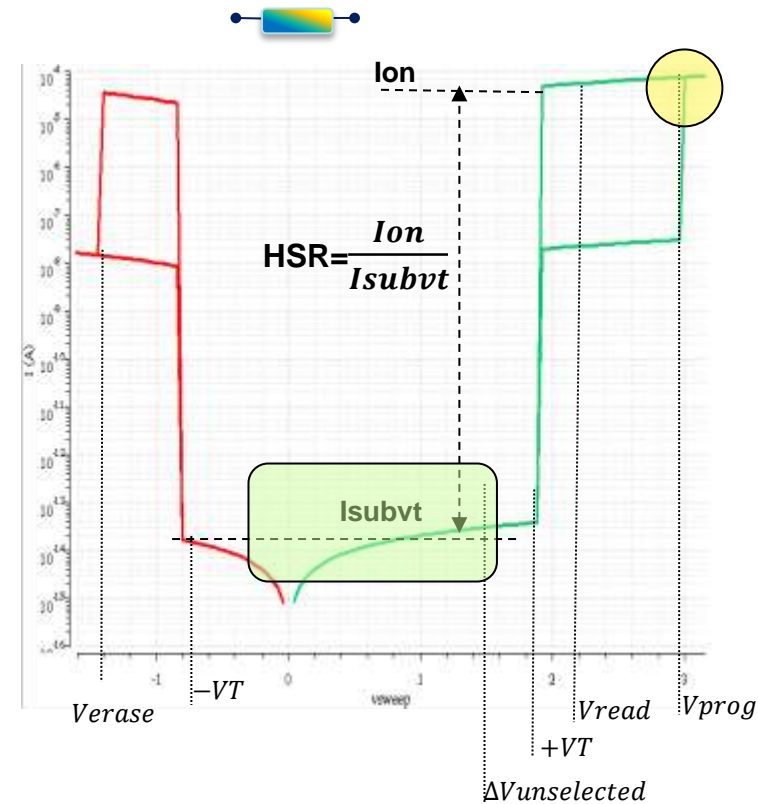
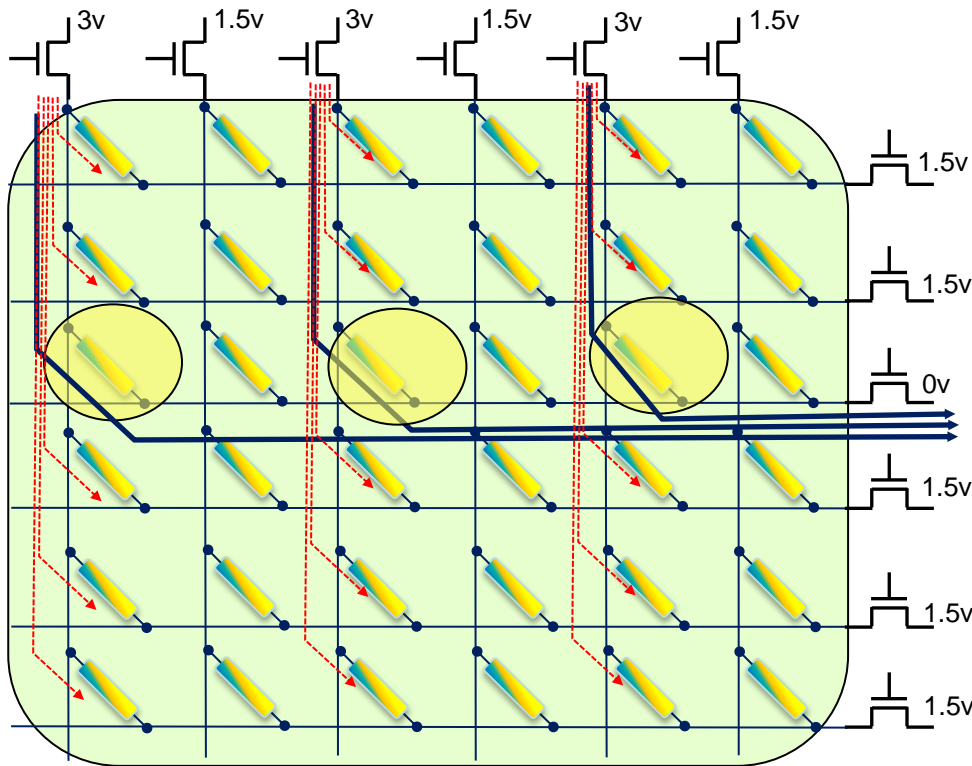


The Sneak Path Barrier with RRAM



- When the array size increases:
 - Programming or Erase power consumption increases – this will demand large decoding transistors and impact silicon area
 - During Read sensing margin will be quickly diminished - $I_{\text{on}}/(I_{\text{off}}+I_{\text{leak}})$ ratio decreases
- Not possible to make high density, high performance, & efficient arrays with linear resistive cells

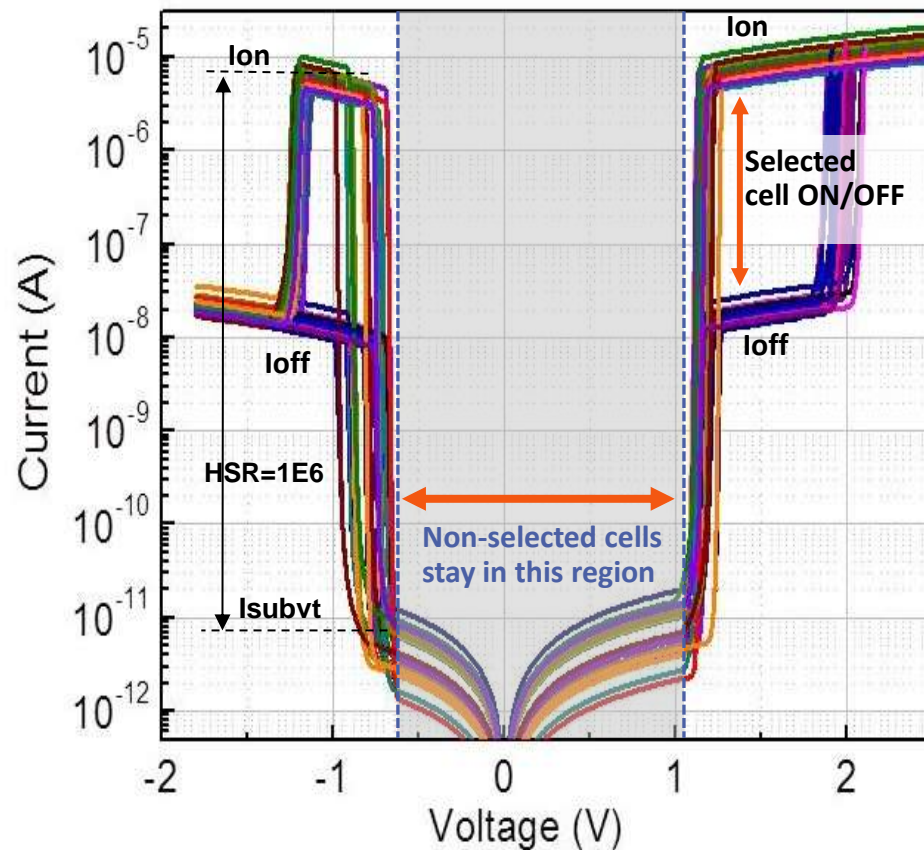
A Non-Linear RRAM with High Selectivity



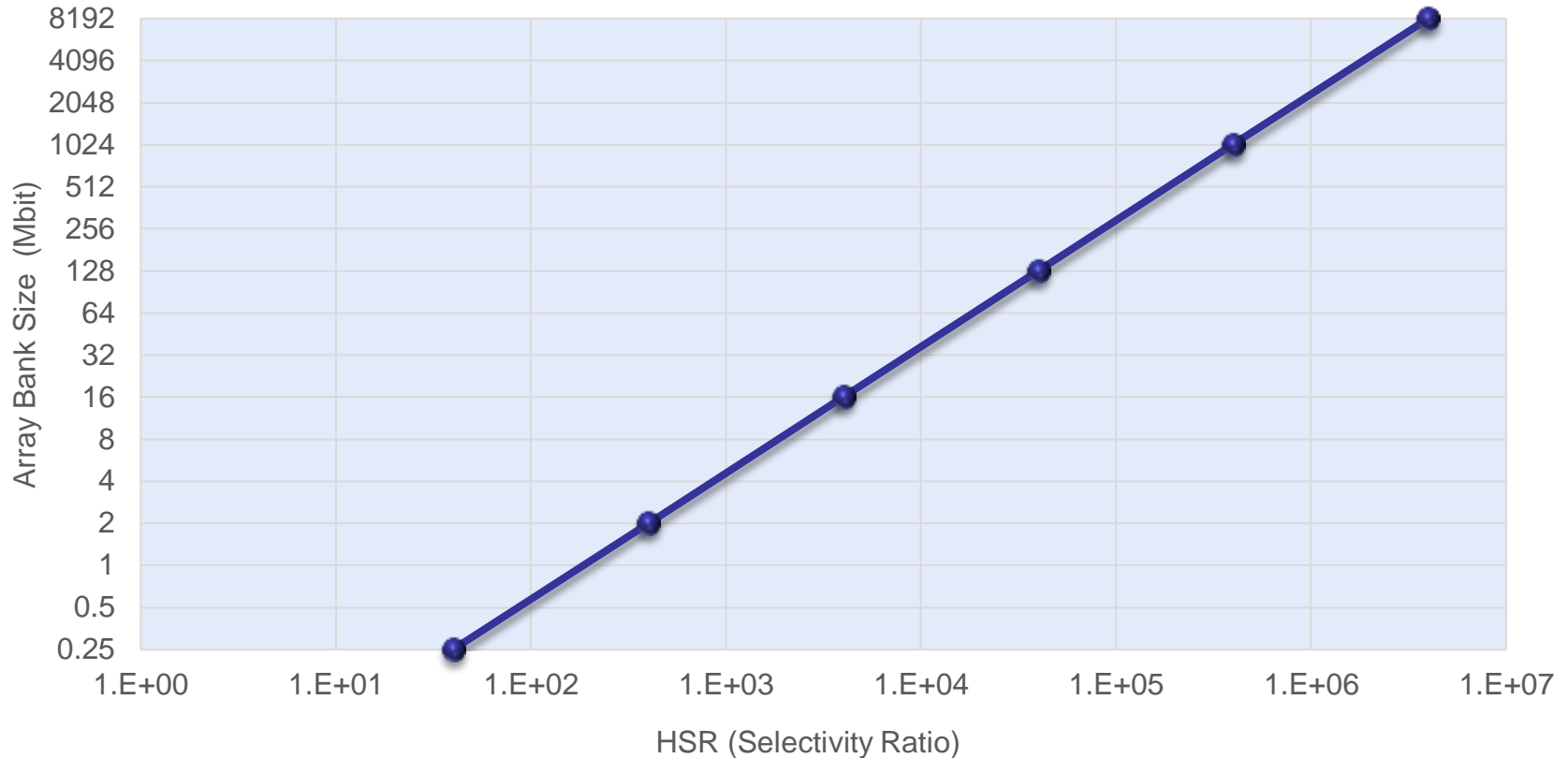
- A device with very high selectivity is needed to suppress the sneak path current in large arrays
- Selectivity feature of the device will activate the cell based on the potential across the two terminal RRAM cell
- Selectivity ratio is measured by HSR (Half Select Ratio)

Crossbar RRAM with Superior Selectivity Ratio

- Crossbar demonstrates a device with an HSR selectivity ratio of $>1E6$
- Eliminates sneak path and provides:
 - **Super high density**
Terabyte devices with 1TnR architecture
 - **Low energy**
write/read operations
 - **High performance**
with very low latency



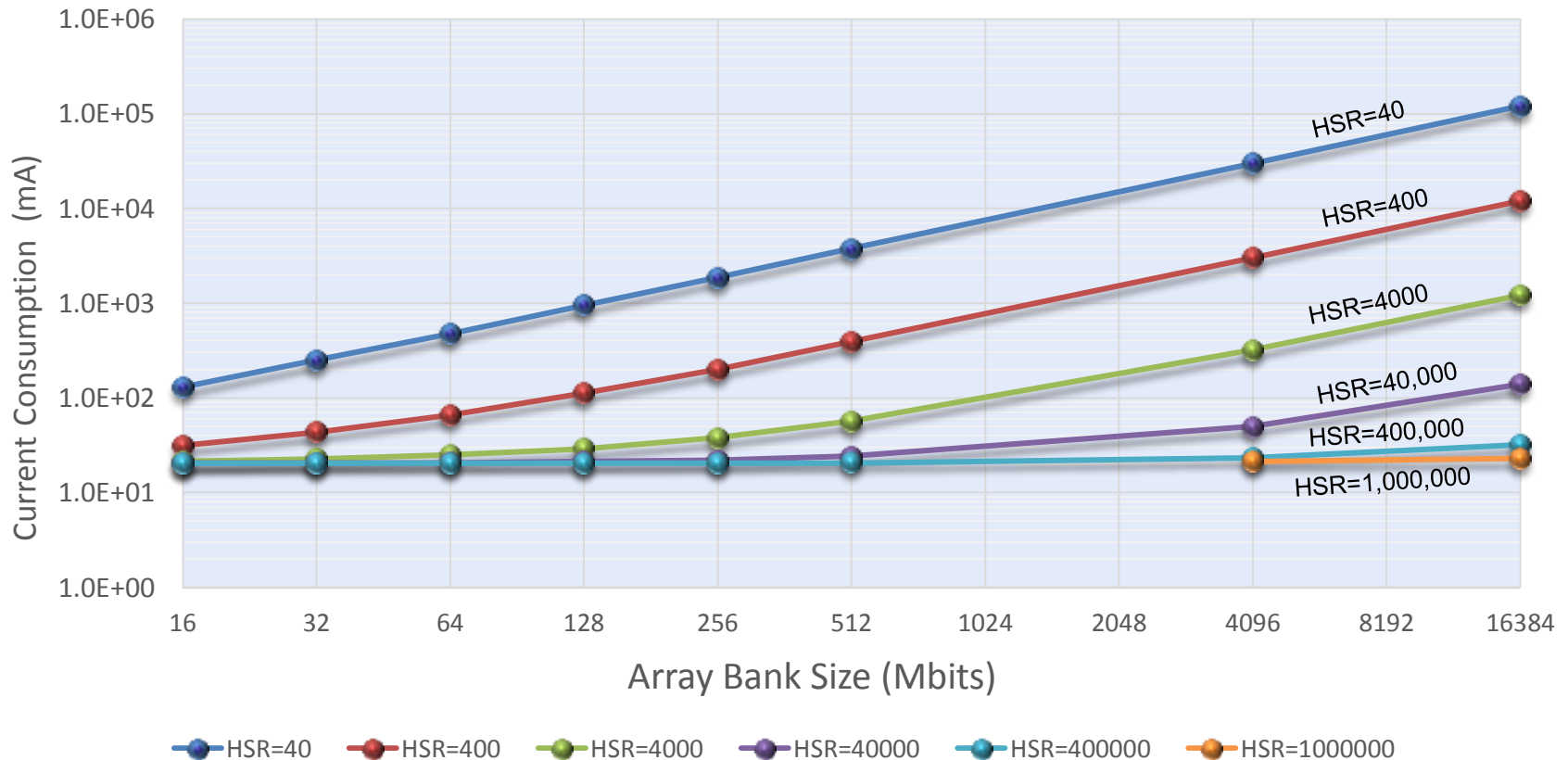
Huge Array Capacity with High HSR



Large HSR enables super high density products with high array efficiency

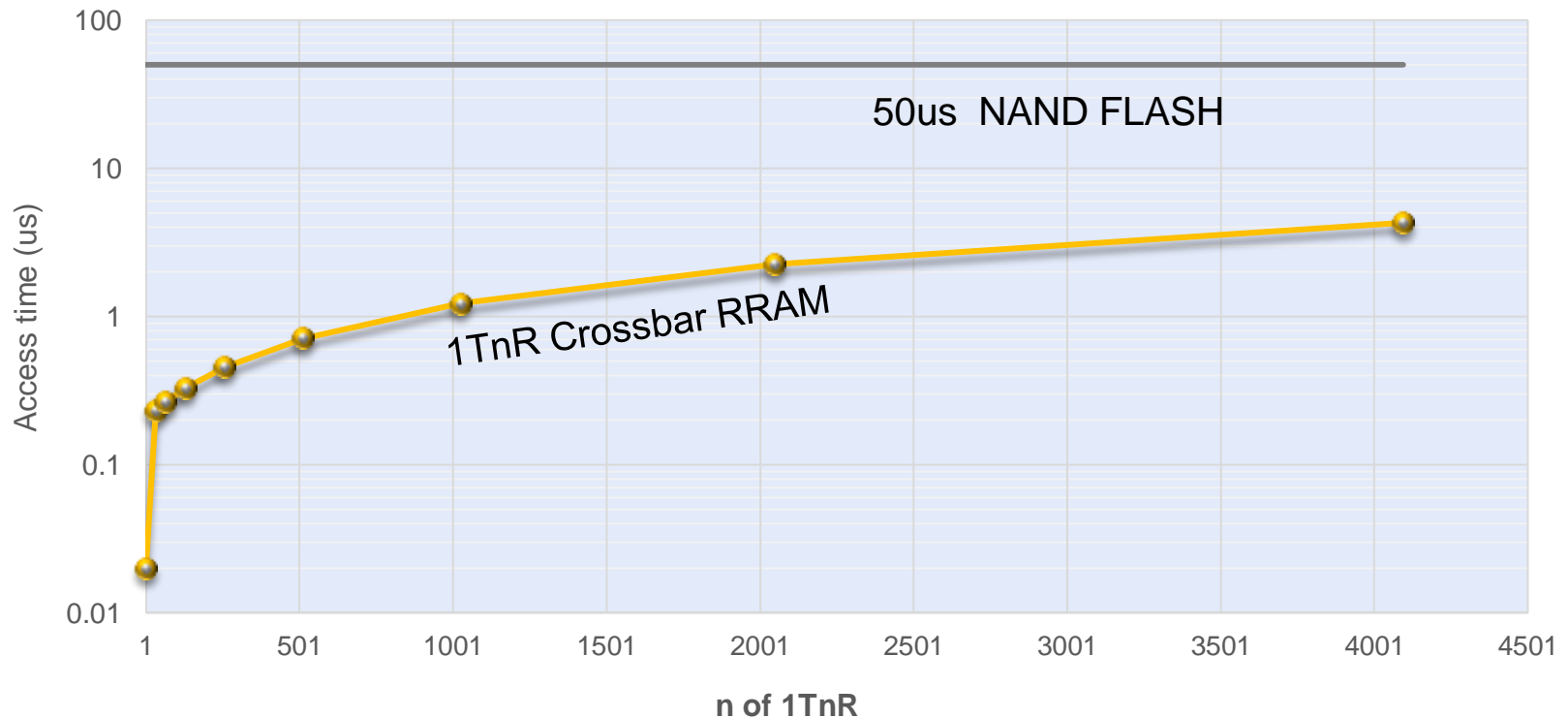
****Requirements: 20mA programming ICC budget with 2048bits program simultaneously**

Low Power Consumption with High HSR



Large HSR enables low power and high density products, significantly reducing the sneak path and power consumption

Superior Performance with High HSR



- Large HSR enables 1TnR architecture suited for high performance high density products
- 25X performance advantage over traditional NAND

- **Crossbar demonstrates RRAM with $>1E6$ selectivity ratio**
- **Crossbar RRAM resolves the Sneak-Path Barrier enabling:**
 - Super high density arrays
 - Low power consumption
 - High performance products
- **All in one product architecture**



Crossbar

