3D ReRAM with Field Assisted Super-Linear Threshold (FAST™) Selector Technology

FOR SUPER DENSE, LOW POWER, LOW LATENCY DATA STORAGE SYSTEMS

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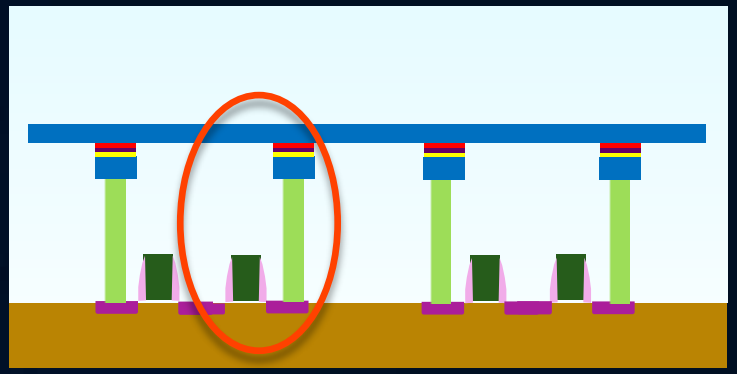
ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE DAC

3D ReRAM FAST™ Selector Technology

- ReRAM Architectures
- ReRAM FAST™ Technology
- ReRAM FAST™ Device Performance
- ReRAM FAST™ System Performance

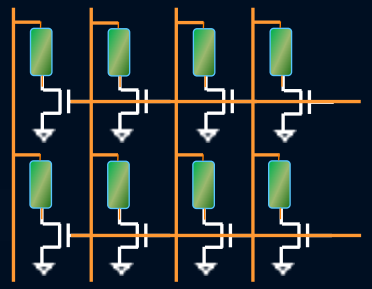
Architectural ReRAM Classification

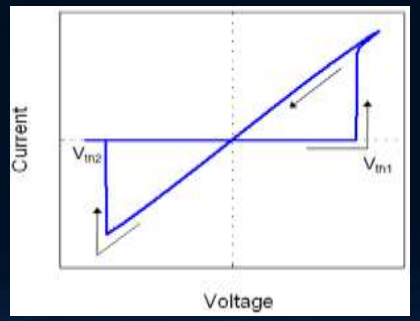
1T1R with Linear ReRAMs



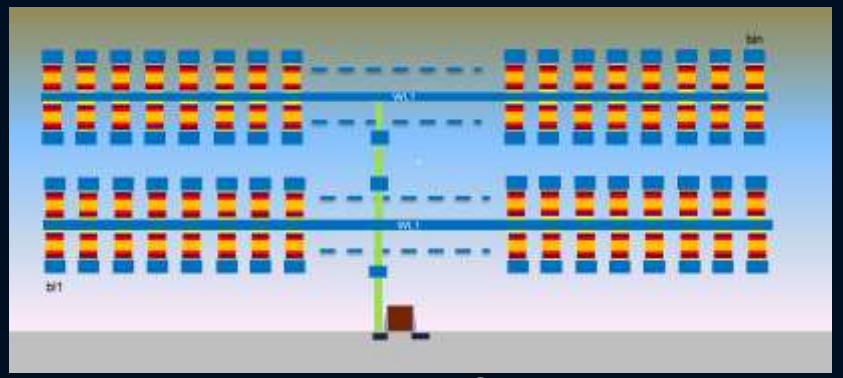
One Select transistor per ReRAM

- Suited for low latency, high speed embedded memory operation or high performance NOR products
- Cell size dominated by the select transistor



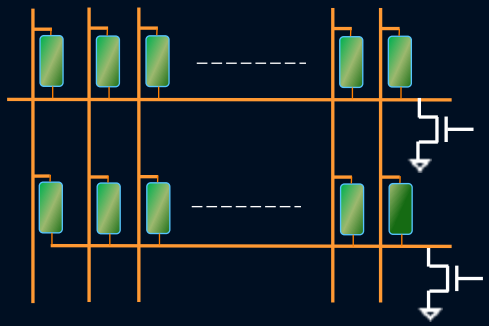


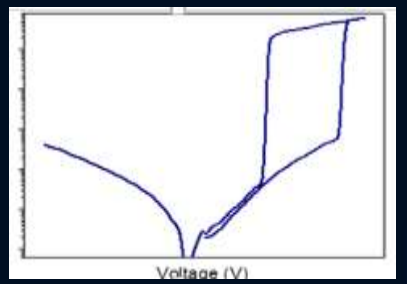
1TnR with Non-Linear ReRAMs



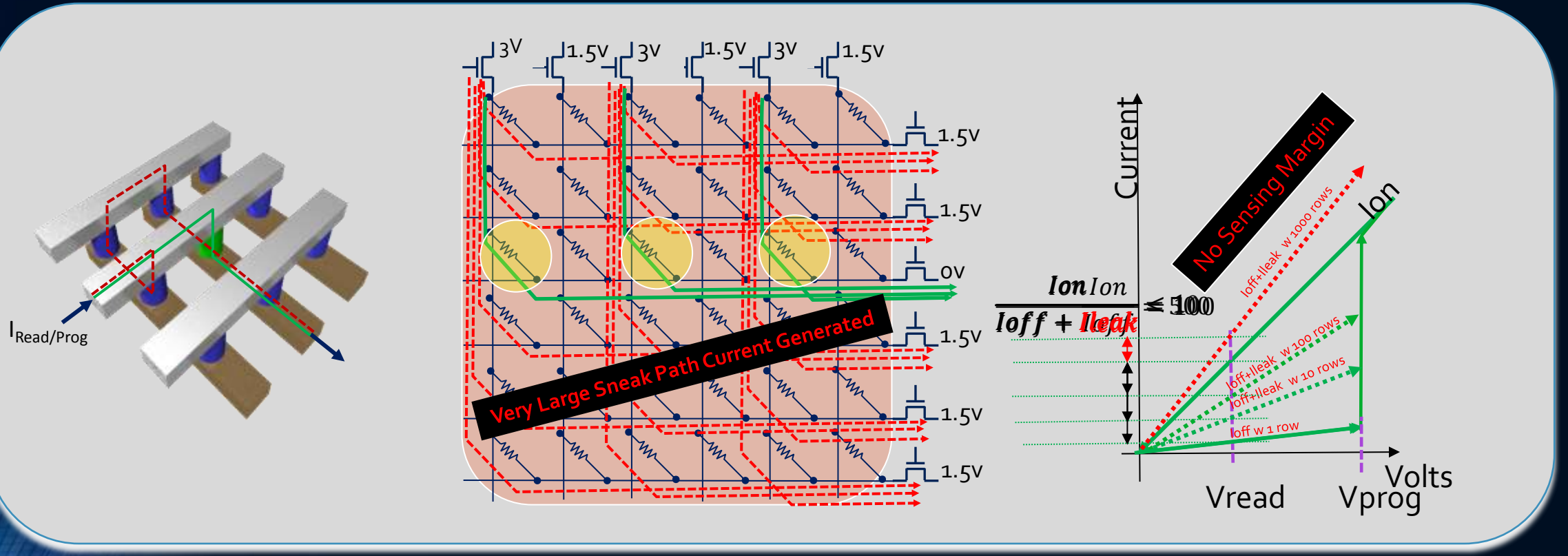
One Access transistor for many ReRAMs

- Suited for high density high performance memory (NAND/SCM memory)
- 3D architecture
- Under array utilized for peripheral circuits yielding high array efficiency
- $Cell\ area = \frac{4F^2}{\#\ RRAM\ Layers}$



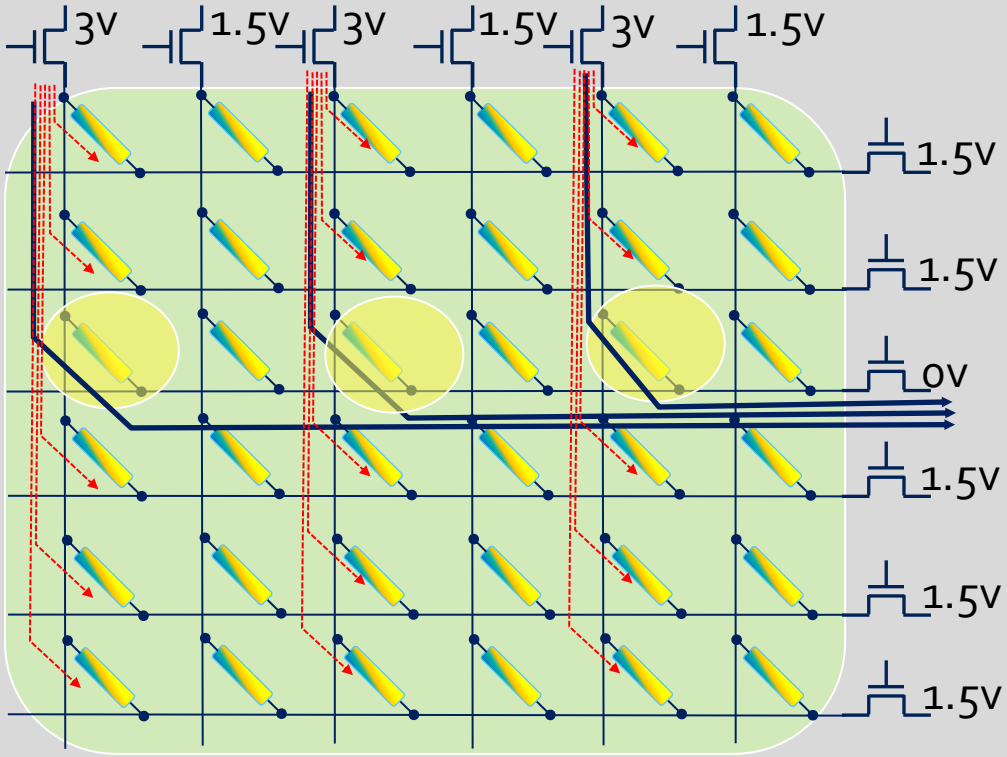


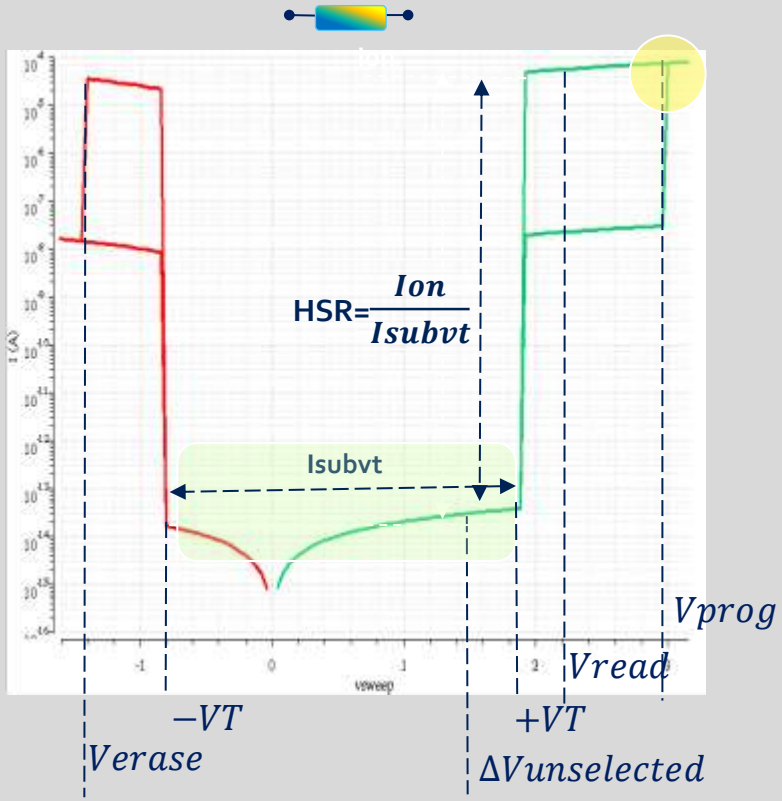
The Sneak Path Issue with ReRAM



- When the array size increases:
  - Programming or Erase power consumption increases – this will demand large decoding transistors and impact silicon area
  - During Read sensing margin will be quickly diminished - Ion/(Ioff+Ileak) ratio decreases
- Not possible to make high density, high performance, & efficient arrays with linear resistive cells

A Non-Linear ReRAM with High Selectivity



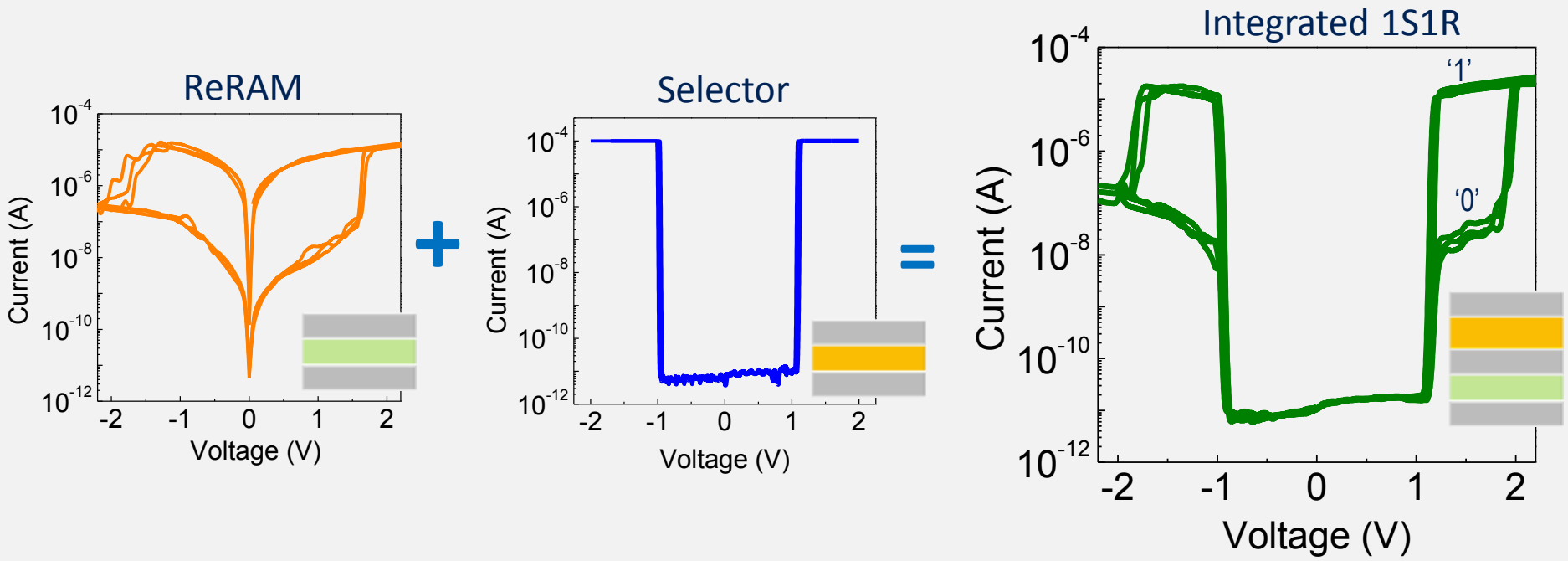


- A device with very high selectivity is needed to suppress the sneak path current in large arrays
- Selectivity feature activates or selects a cell based on the potential across the ReRAM cell
- Selectivity ratio is measured by HSR (Half Select Ratio)

ReRAM FAST™ Selector Technology Characteristics

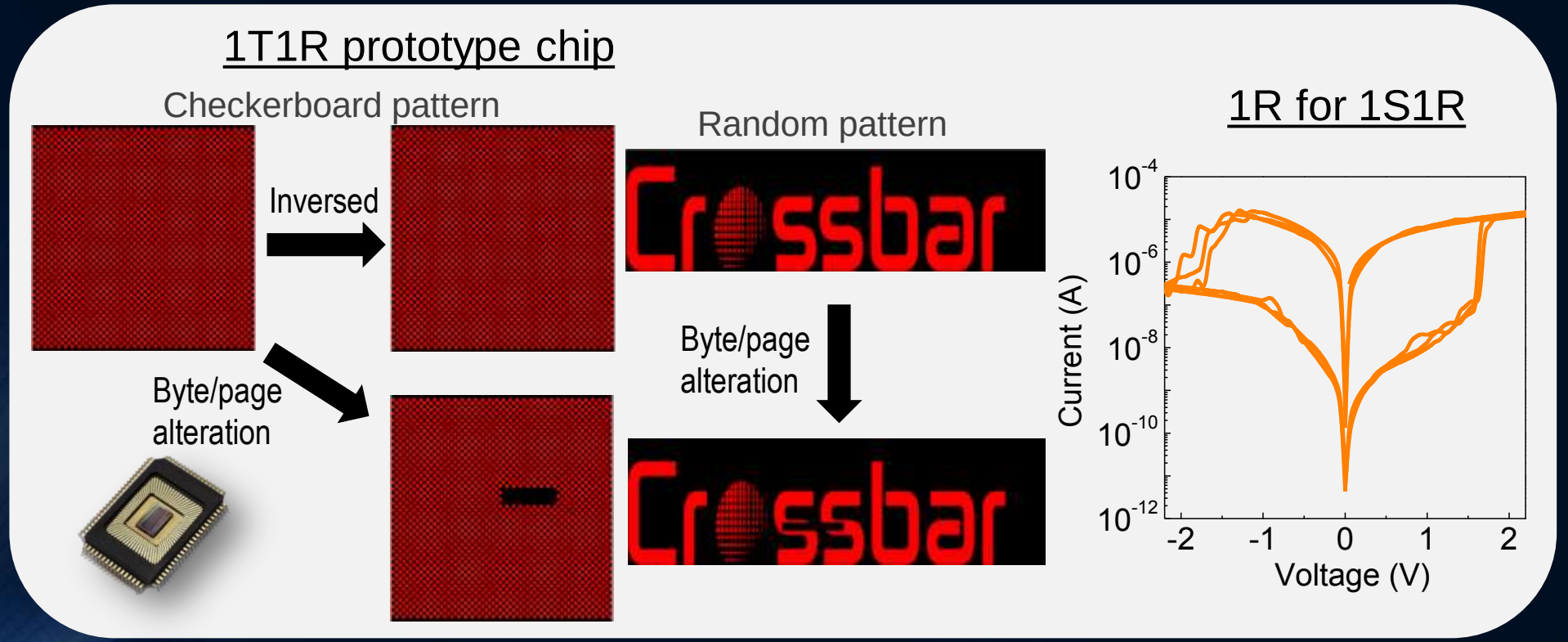
ReRAM + Selector (1S1R)

- Cross-point array integration of ReRAM + Selector
  - High HSR & sharp switching slope of a selector
  - Small voltage overhead for selector integration



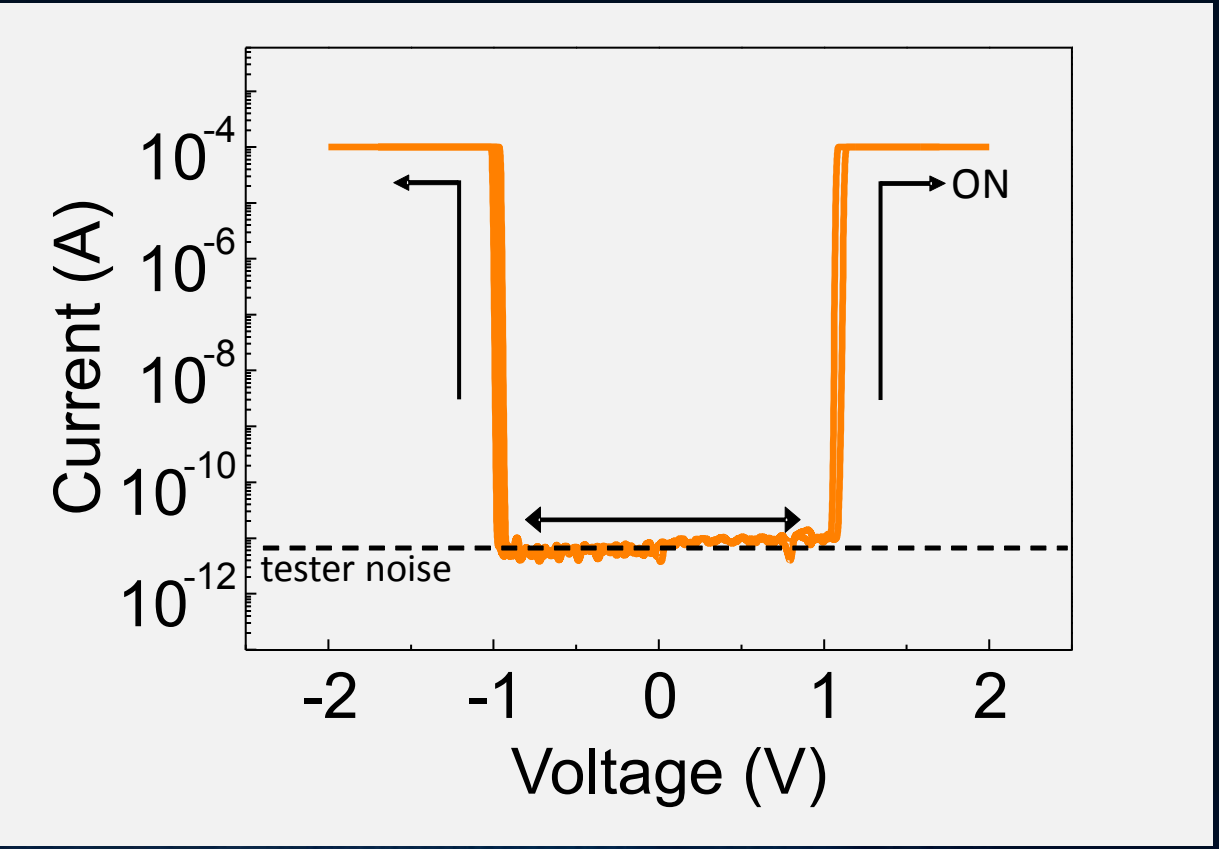
ReRAM 1R Component

- Used 1R from one of Crossbar's 1T1R technologies
- No high voltage forming process required



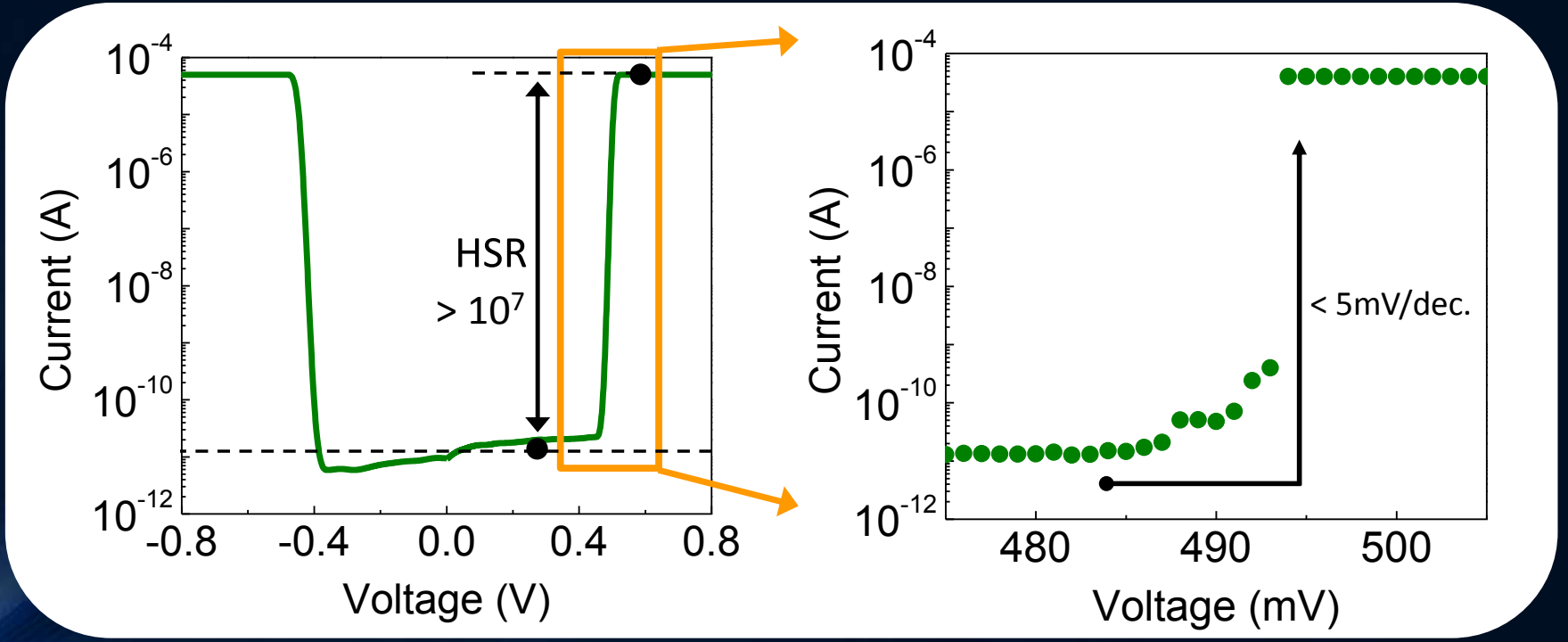
FAST™ Selector Component

- Utilizes an oxide-based Super-Liner Threshold (SLT) layer
- Bidirectional volatile on-off operation (E-field assisted)
  - Ideal for bipolar ReRAM
  - Formation of volatile percolation paths in SLT select layer at V_{TH}



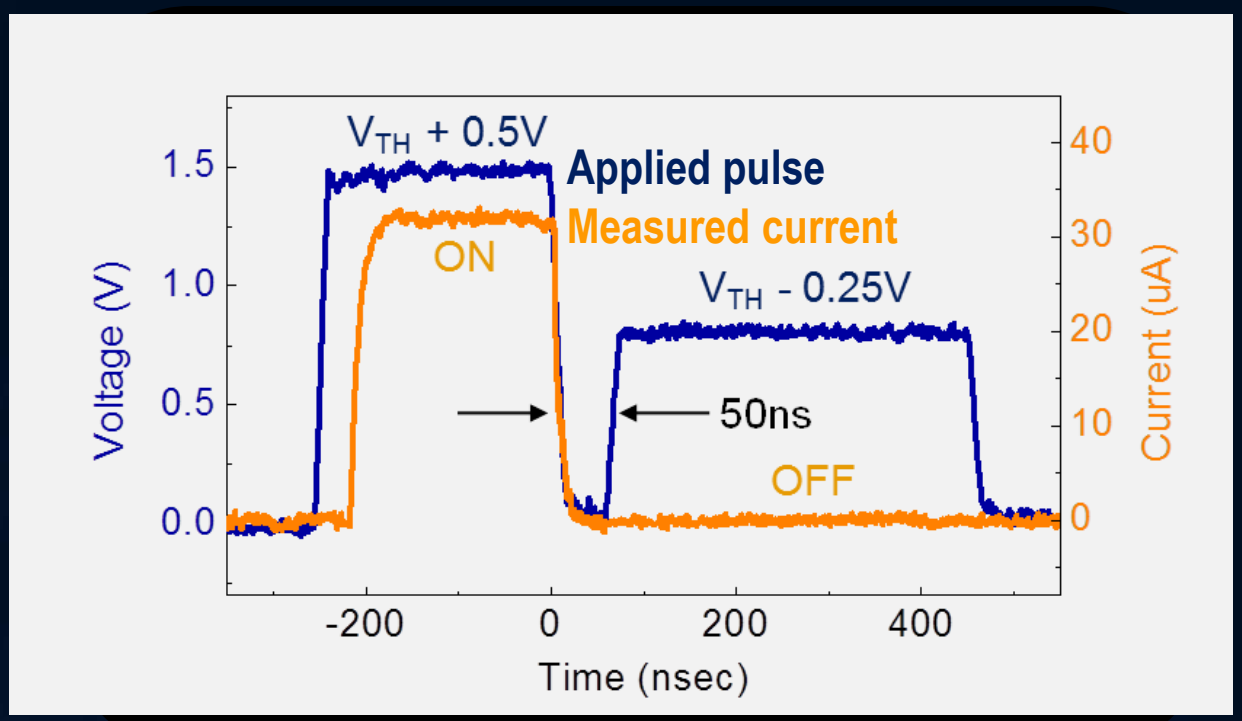
Selectivity (HSR) & Switching Slope

- Half Select Ratio (HSR, $I_{@V}/I_{@0.5V}$) of > 10^7
  - Enables larger array & reduced power consumption
- Extremely sharp switching of < 5mV/dec.
  - Offers more read voltage margin & faster read



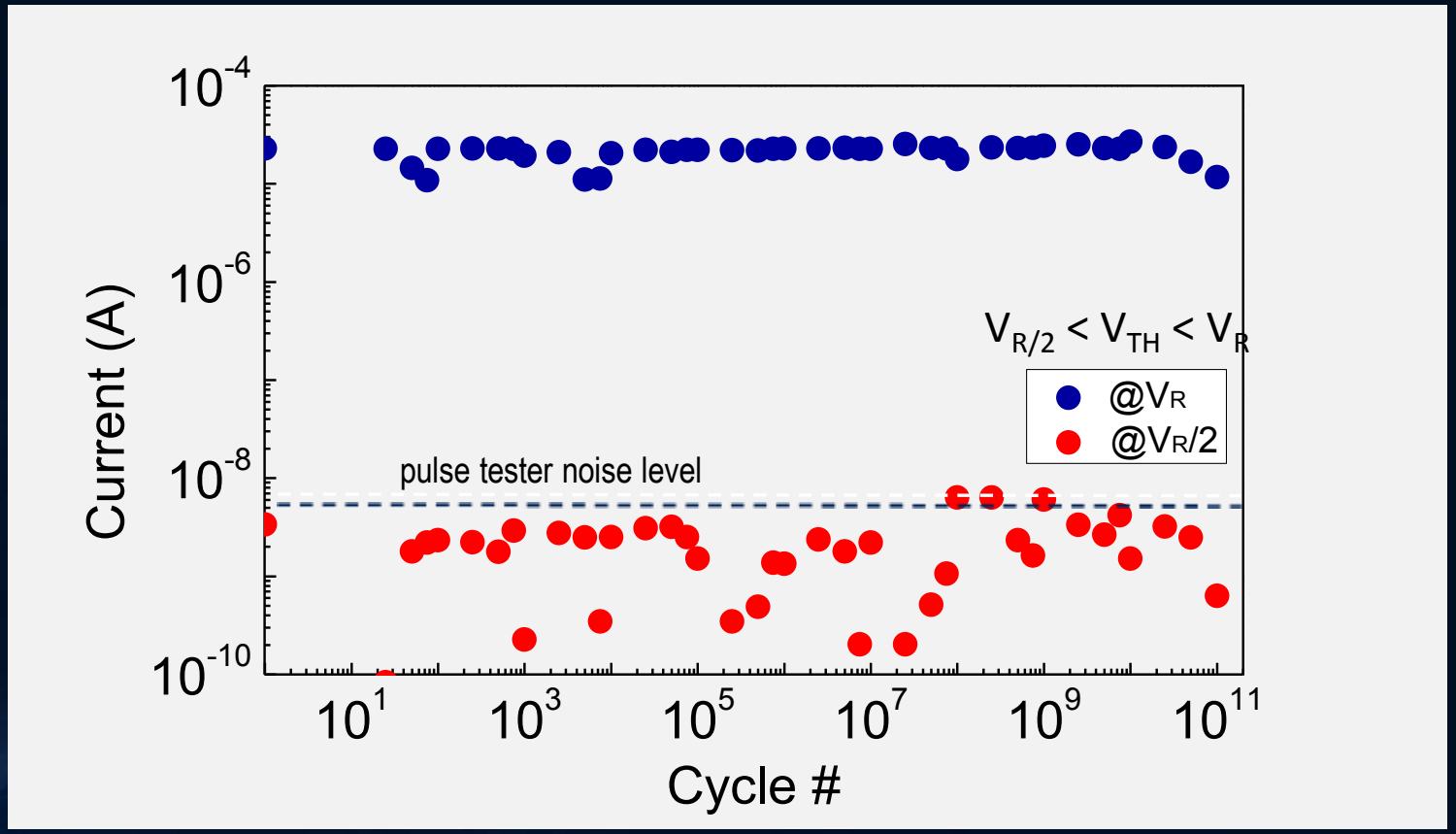
Volatile Selector Switching

- Sub-50ns volatile switching and recovery times
  - Conducting state @ $V > V_{TH}$
  - Insulating state @ $V < V_{TH}$



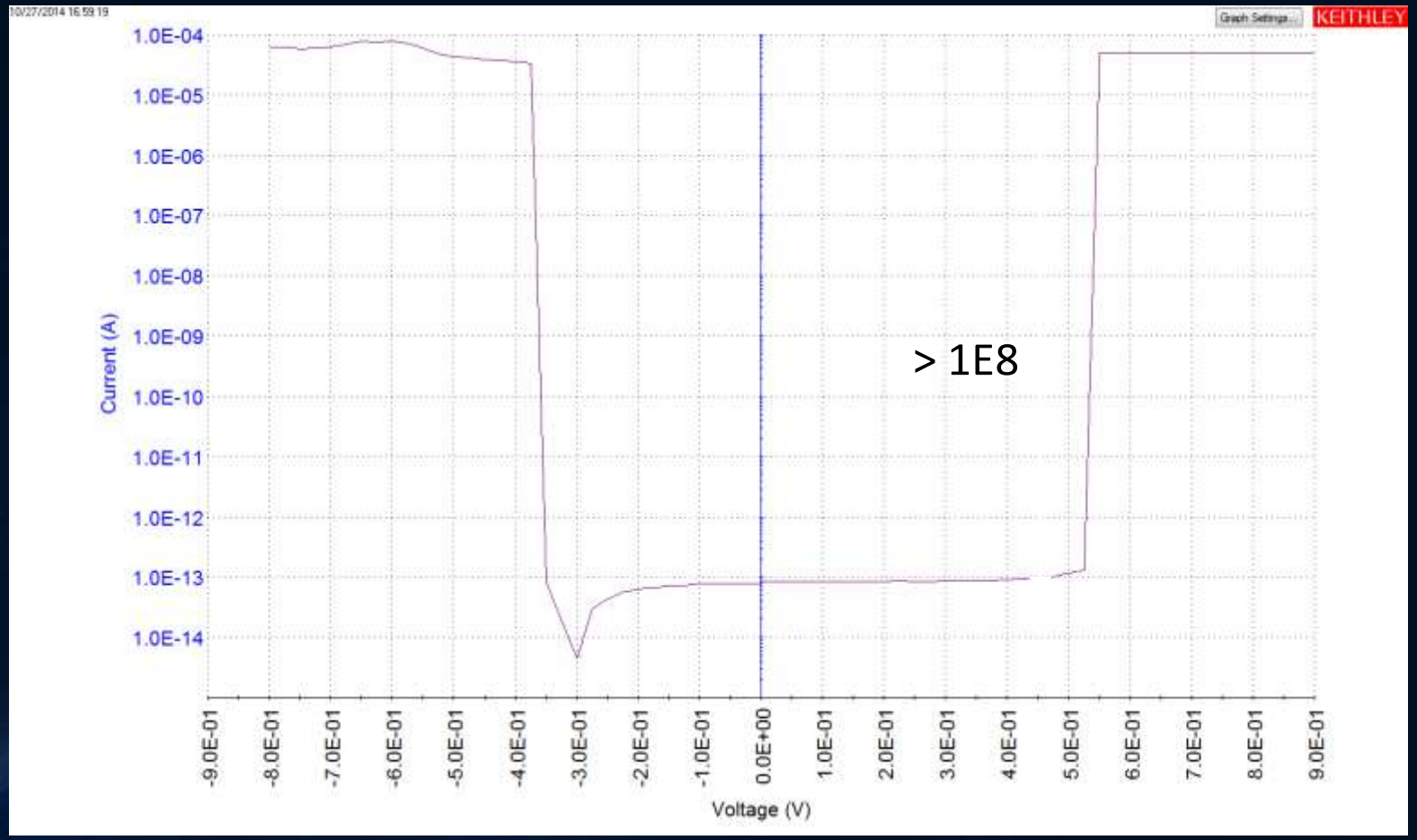
Selector Cycling

- Reliable switching over 10^{11} cycles



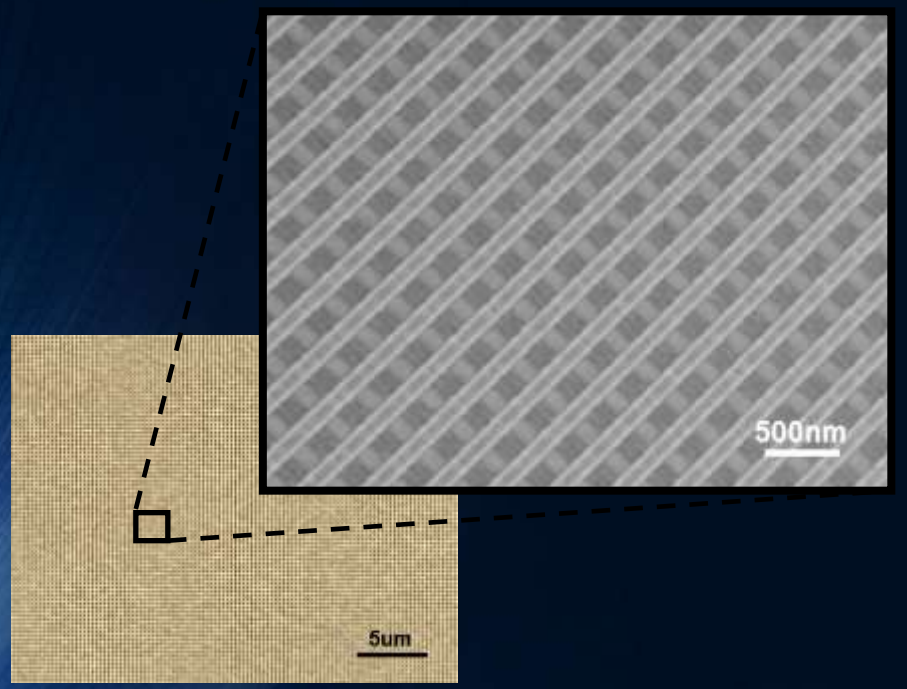
Selector Leakage Current

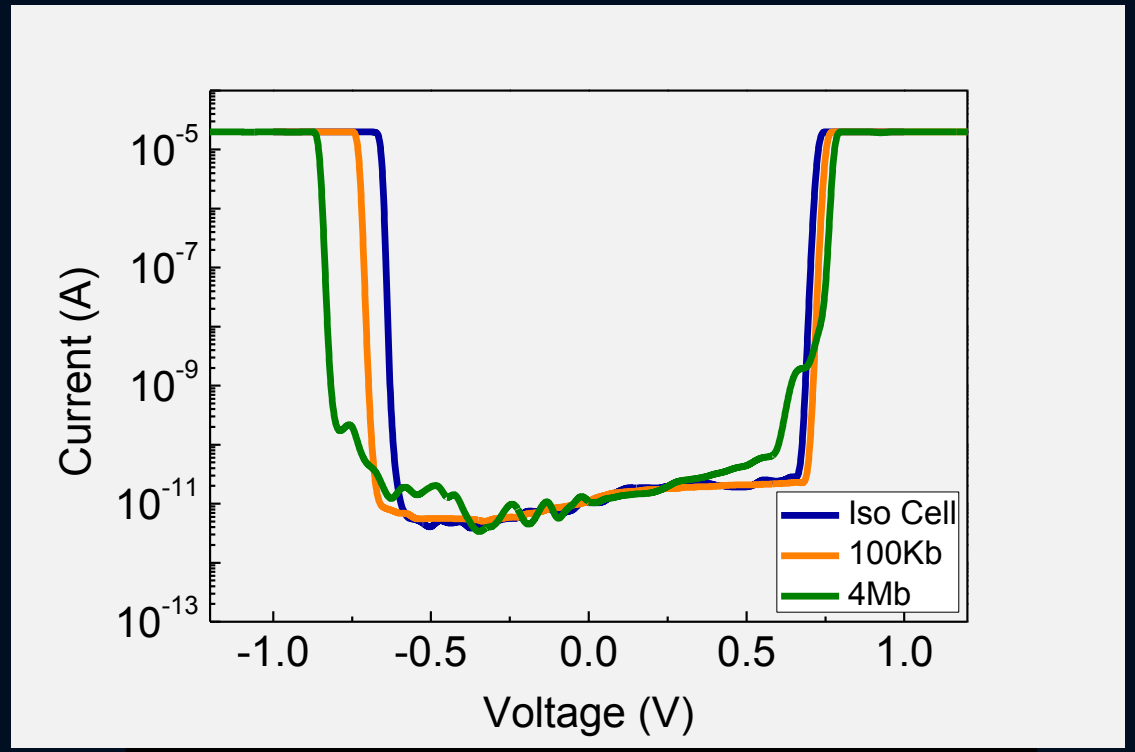
- Low noise measurement confirmed the leakage current less than 0.1pA



Selector Arrays

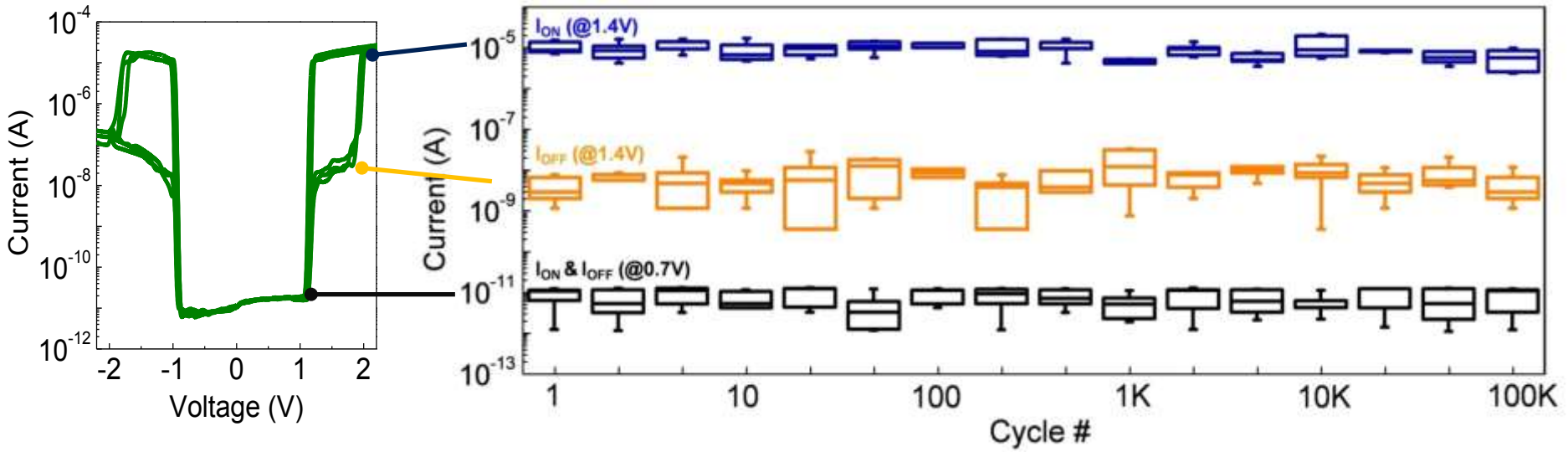
- Suppression of leakage current confirmed in 4Mb cross-point selector array





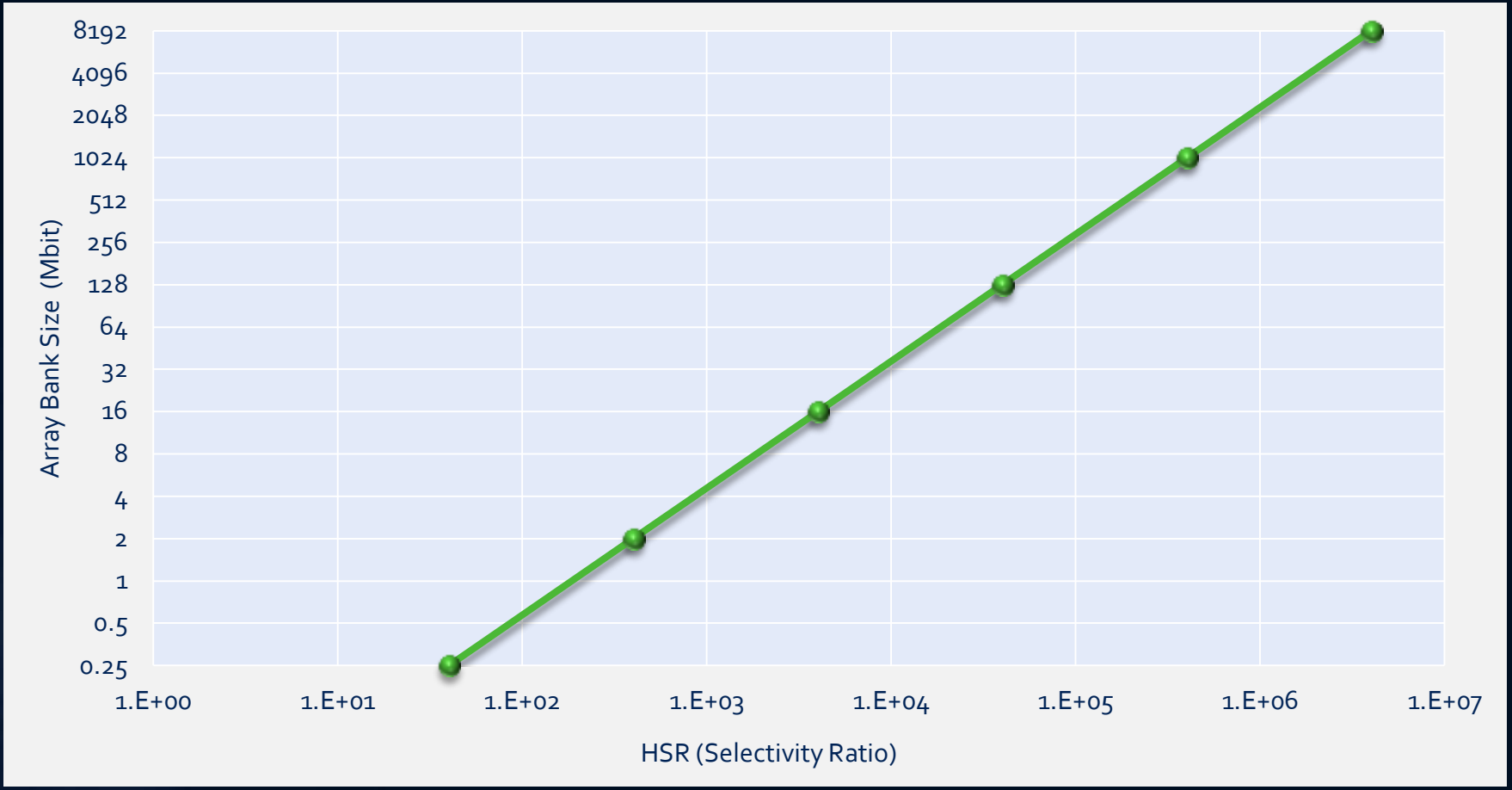
1S1R Cycling

- 1S1R cycling demonstration with large on/off memory ratio and selectivity



ReRAM + FAST™ Device Performance

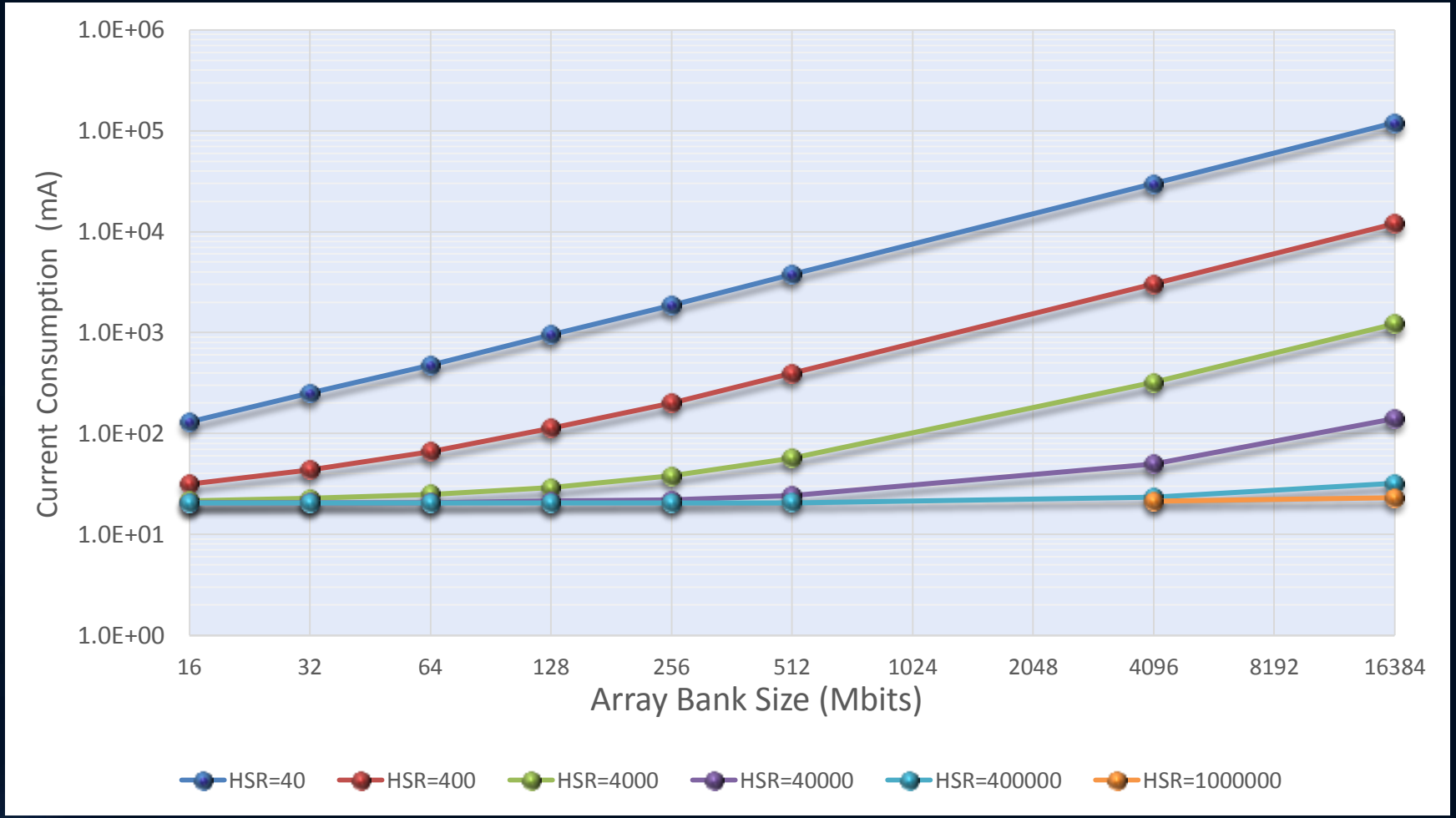
Huge Array Capacity Enabled by High HSR



Large HSR enables super high density products with high array efficiency

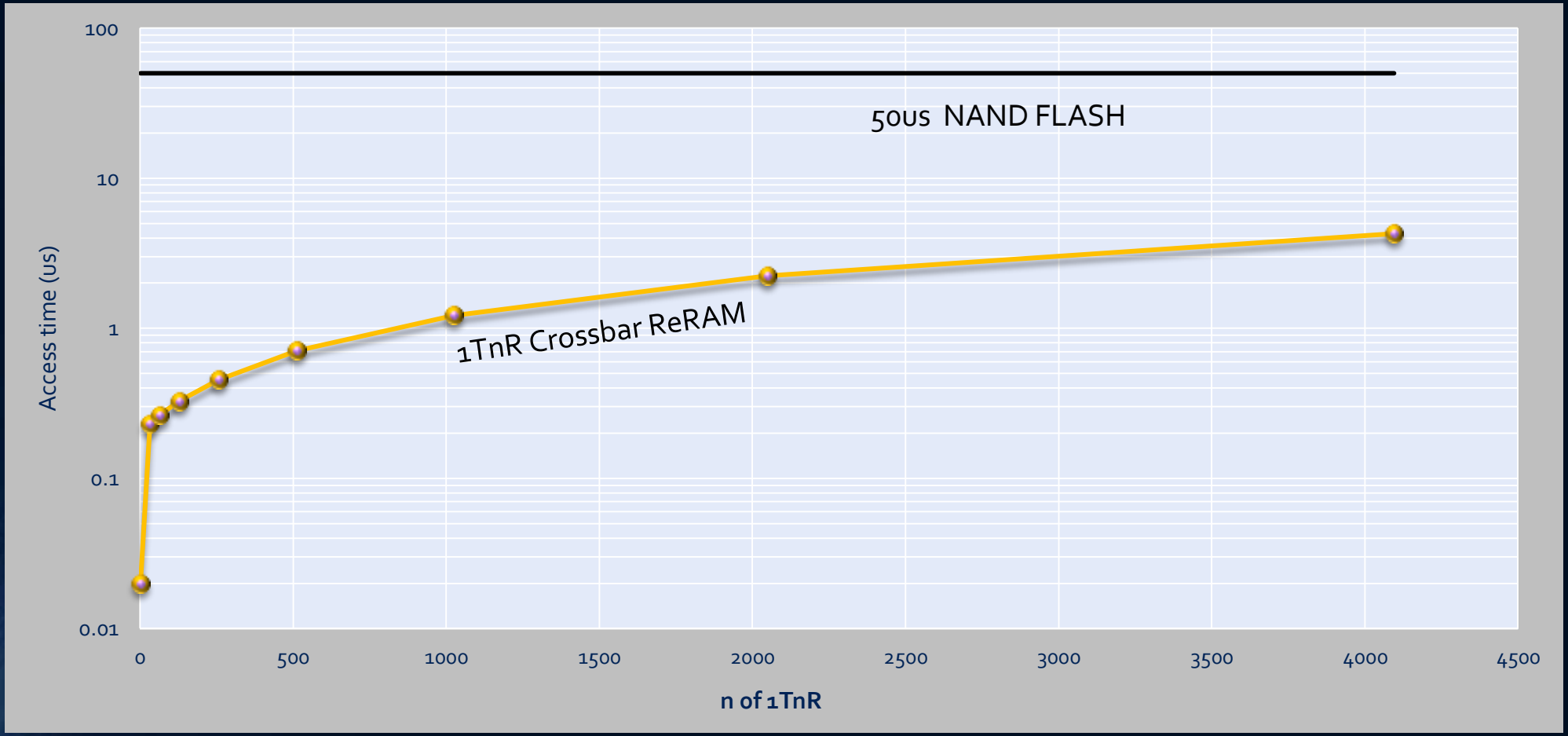
**Requirements: 20mA programming ICC budget with 2048bits program simultaneously

Low Power Consumption Enabled by High HSR



Large HSR enables low power and high density products, significantly reducing the sneak path and power consumption

Superior Performance Enabled by High HSR



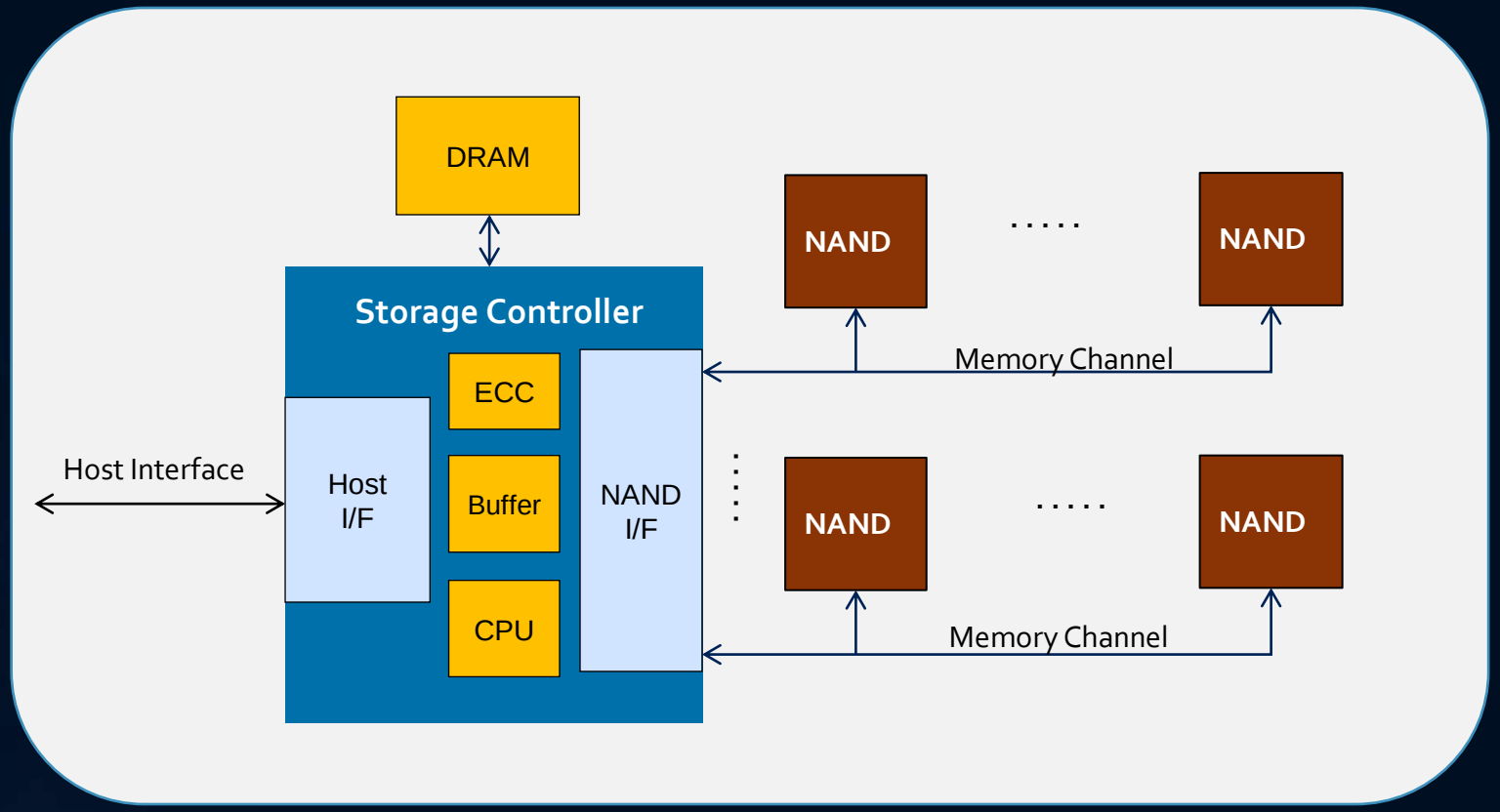
- Large HSR enables 1TnR architecture suited for high performance high density products
- 25X performance advantage over traditional NAND

Existing NV Memory Technology Comparison

Feature	NOR	NAND	ReRAM
Non-Volatility	Yes	Yes	Yes
Random Read Time	90ns -100ns	50us	70ns - NOR **1us - NAND**
Byte Write **Page Write**	NO Program page/byte Erase large sector	No Program page Erase large sector	**Yes, Overwrite** **Yes, Overwrite**
Write/Program Time	700us/256B	>1000us /8KB (MLC)	64us/8KB 16us/2KB **2us/Byte**
Erase Time/Size	30ms/4KB	>2ms(Block)	Not required
Endurance	10^5	MLC 10^3	**10^8 - 10^{12}**
Cell Size **MLC/Stacking**	6-8F^2 MLC	SLC 5F^2 MLC	**SLC 4F^2** **Stacking, MLC**
Cost	Med	Low	Very Low

Storage System Performance

SSD System NAND-Based



NAND Shortcomings: L2P Mapping, Garbage Collection, Wear Leveling, Bad Block Management, ECC Complexity

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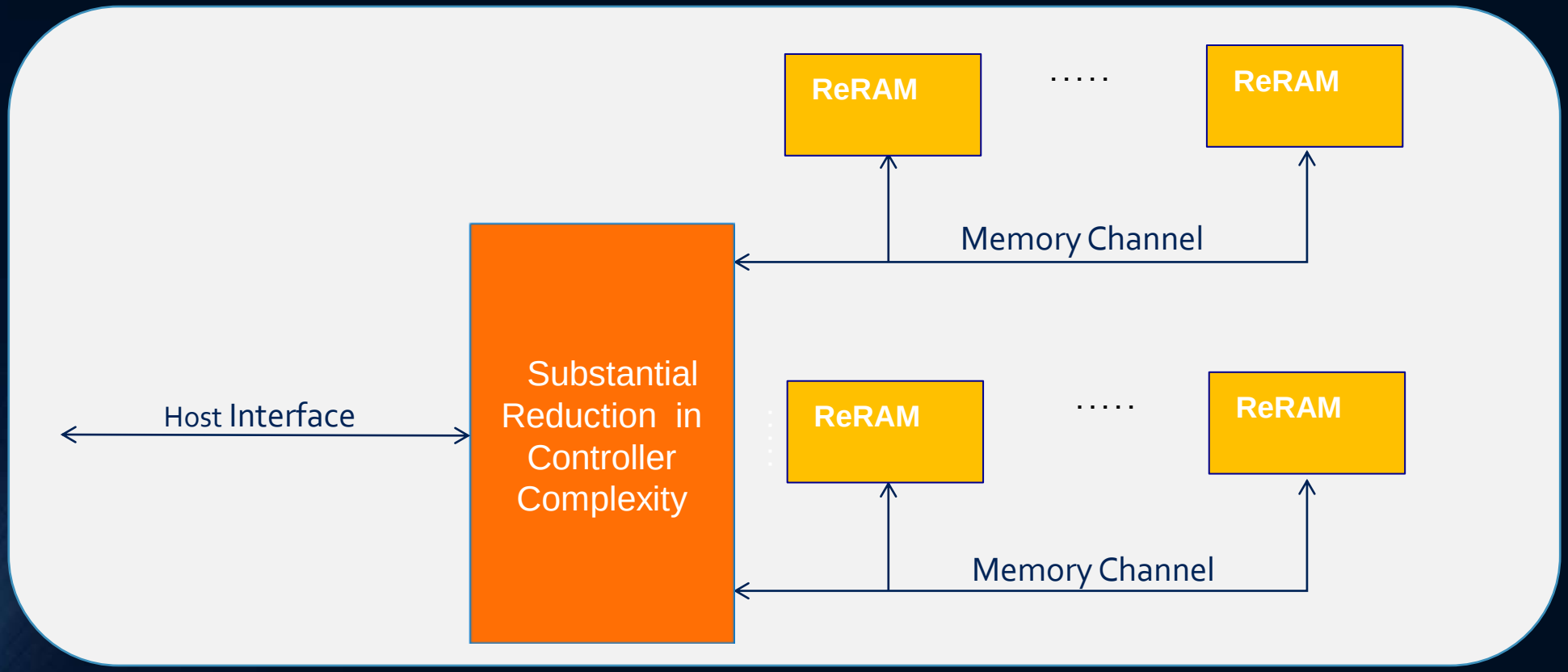
SSD System ReRAM-Based



ReRAM-Based SSD substantially reduces NAND shortcomings, thus significantly reducing controller complexity

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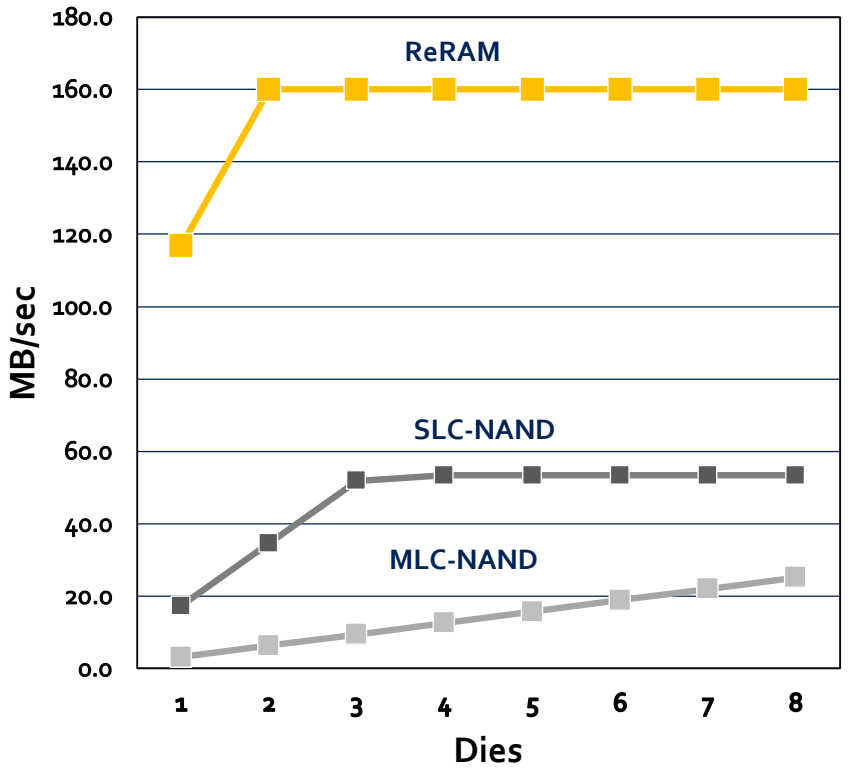
SSD System Performance with NAND & ReRAM

NAND Spec.	MLC	SLC	ReRAM
NAND bus freq DDR (MHz)	100	100	100
Bus width (bits)	8	8	8
Page Size (KB)	16	16	4
Shift Time + Overhead (us)	100	100	25
Program Time (ms)	1.5	0.3	.032
Read Latency (us)	50	25	1
Write Amplification	3	2	1
Effective Write xfer rate (MB/s)	32	53	160



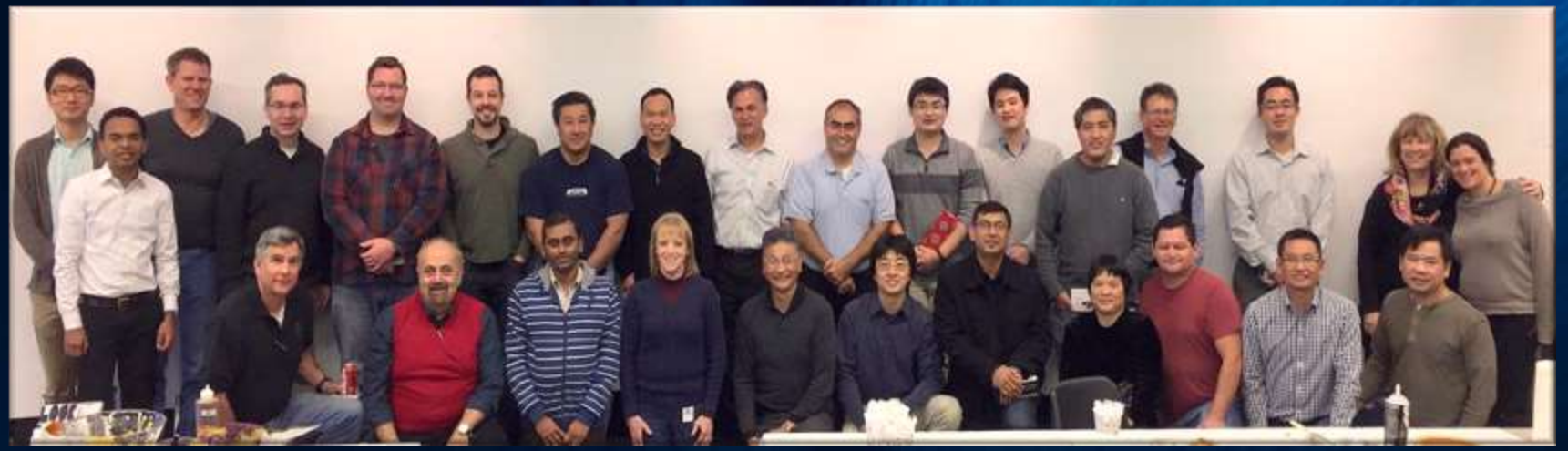
- ReRAM utilizes the Maximum Bandwidth of the channel
- ReRAM provides at least 5X performance improvement

- Crossbar demonstrates The FAST™ device with selectivity ratio of >1E6

- FAST+ReRAM based products provide superior performance and architectural flexibility enabling storage systems with:
  - **Super high density**
    Terabyte devices with 1TnR architecture
  - **Low energy**
    write/read operations
  - **High performance**
    with very low latency
  - **Simplified Software and Hardware infrastructure**

Acknowledgements

CROSSBAR TEAM



For further information on Crossbar's technology, visit us at
www.crossbar-inc.com